Instrument Data Processing Unit for THEMIS

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Abstract The Time History of Events and Macroscale Interactions during Substorms
(THEMIS) mission is a NASA Medium-class Explorer (MIDEX) mission, launched on February 17, 2007. The mission employs five identical micro-satellites, or "probes," which line-up along the Earth's magnetotail every four days in conjunctions to determine the trigger and
large-scale evolution of magnetic substorms. The probes are equipped with a comprehensive
suite of instruments that measure and track the motion of thermal and super-thermal ions and
electrons, and electric and magnetic fields, at key regions in the magnetosphere. Primary science objectives require high data rates at periods of scientific interest, large data volumes,
and control of science data collection on suborbital time scales. A central Instrument Data
Processing Unit (IDPU) is necessary to organize and prioritize the data from the large number of instruments into a 200 MB solid state memory. The large data volume produced by
the instruments requires a flexible memory capable of both high resolution snapshots during
conjunctions and coarser survey data collection throughout the orbit. Onboard triggering
algorithms select and prioritize the snapshots based on data quality to optimize the science
data that is returned to the ground. This paper presents a detailed discussion of the hardware
and software design of the THEMIS IDPU, describing the heritage design that has been
fundamental to the THEMIS mission success so far.

1 Introduction

The Time History of Events and Macroscale Interactions during Substorms (THEMIS) mission, the fifth NASA Medium-class Explorer (MIDEX), launched on February 17, 2007 to
determine the onset and large-scale evolution of substorms. Flying in synchronous orbits

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within the earth's magnetosphere, the five THEMIS satellites, or Probes, track the particle and field processes responsible for eruptions of the aurora. A simple Instrument Data Processing Unit (IDPU) manages the entire instrument suite, collecting and organizing the data before transmission to the ground. The IDPU controls a large number of instruments: 2 Solid State Telescopes (SSTs), 1 Electrostatic Analyzer (ESA), 6 Electric Field Instruments (EFIs), 1 Search Coil Magnetometer (SCM) and 1 Flux Gate Magnetometer (FGM). It also performs critical actuator and deployment tasks such as wire boom deployments (4 per Probe), rigid boom deployments (4 per Probe), one-shot cover openings (1 per Probe) and attenuator control (2 per Probe) (see Pankow et al. 2008). In addition, support electronics include instrument signal conditioning, power control and distribution, command routing, data optimization and analysis, and housekeeping monitoring.

The high resolution science data required during scientifically interesting events drove a design philosophy to autonomously change data rates based on parameters of interest, or "trigger" functions. To accommodate the different data rates, the THEMIS team developed four levels of data collection: Slow Survey, Fast Survey, Particle Burst and Wave Burst. The IDPU controls the data collection rates based upon trigger data, and prioritizes the high resolution burst data for selective transmission to the ground. To reduce the work load on the low-power 8085 IDPU processor, numerous tasks normally performed by a processor were delegated to custom designed circuits using Field Programmable Gate Arrays (FPGAs). The IDPU software is then able to focus on data prioritization and compression schemes to maximize the quality and quantity of the science data. This data optimization scheme has led to high value, scientifically interesting data being collected and downlinked every orbit.

The IDPU circuitry is packaged in a single box to reduce mass, to simplify harnessing and interfaces, and to reduce duplication in power converters and other common services. Electronic parts for the IDPU were selected according to criteria for low-power, functionality, reliability, and radiation hardness. Moderate part reliability levels (to MIDEX standards) were coupled with extensive board and instrument-level testing to assure reliability. Parts were specified to and/or lot tested and shielded to achieve a minimum total dose radiation tolerance requirement of 66 Krads.

This paper is organized into two main sections providing a detailed discussion of the hardware and software design of the THEMIS IDPU.

2 Hardware Description

The IDPU consists of a 7-slot 6U VME chassis. The IDPU hardware boards can be grouped into two main functions: core electronics boards including a Data Controller Board (DCB), Low Voltage Power Supply (LVPS), and Power Controller Board (PCB); and instrument specific support boards including a Digital Fields Board (DFB), Boom Electronics Board (BEB), Fluxgate Magnetometer Electronics (FGE), ESA/SST Interface Circuit (ETC), and SST Instrument Digital to Analog Processing Board (DAP). The DCB collects, formats, frames, and stores data from the instrument specific boards and then sends it to the Probe's C&DH processor in the Bus Avionics Unit (BAU) for transmission to ground. It also accepts commands from the BAU and controls instrument operations. The solid state recorder (SSR), resident on the DCB, is a 200 MB error-corrected SDRAM that can be configured to store multiple data types (survey, burst) and data rates up to 630 Kbps. The power system (LVPS and PCB) provides stable, regulated voltages through DC/DC conversion to the instrument support boards and sensors. The LVPS, connected to the VME Chassis through a Hypertronics connector, conditions and converts probe power for the instrument electronics and mechanisms. The PCB monitors current draw and voltages, switches instrument
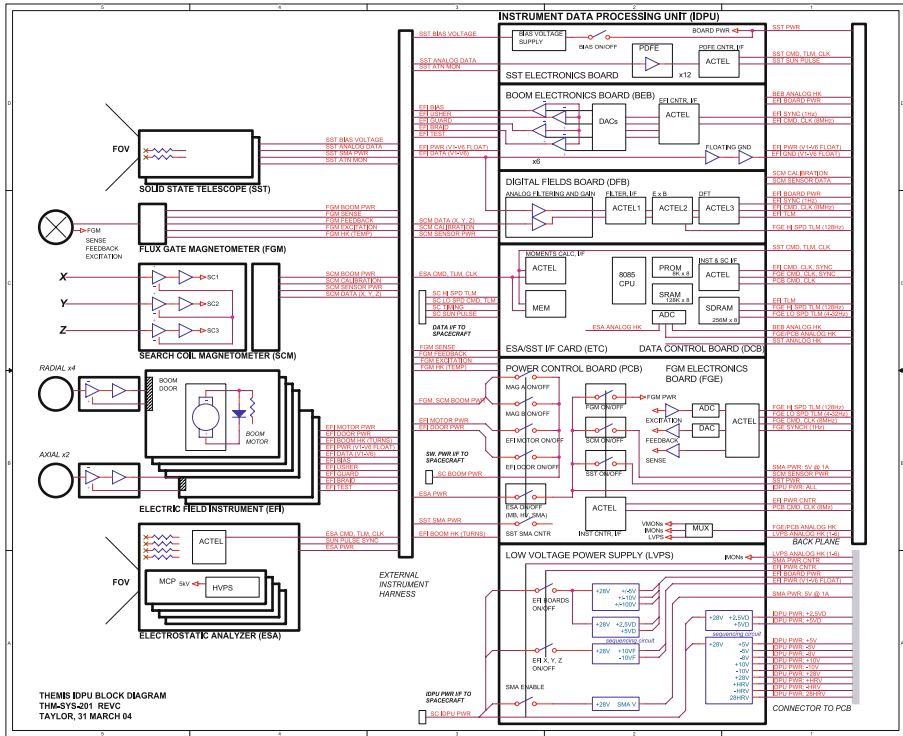
Fig. 1 THEMIS IDPU block diagram

power services, and provides current limiting. The instrument support boards (DFB, BEB, FGE, ETC, and DAP) collect and condition instrument specific data. The instrument support boards are briefly described here and more extensively in separate papers (Auster et al. 2008; Bonnell et al. 2008; Cully et al. 2008; Larson et al. 2008; McFadden et al. 2008). Figure 1 shows a detailed block diagram of the IDPU.

The IDPU has a number of independent operating configurations, which mainly affect instrument science data accumulation rates. Only three basic modes (Safe, Low Power, and Science Mode) affect power consumption and dissipation. A fourth mode, Engineering Mode, affects the IDPU housekeeping data rate only. In Safe Mode, only the core systems are powered. This mode is entered on reset (power-on), by a ground command, or in response to a flag in the spacecraft computer signaling that power is imminent. Safe Mode preserves power to and saves the contents of the SSR. In Low Power Mode, the core system and the FGM are powered on, but all other instruments are off. This mode is entered by a ground command in preparation for maneuvers, as FGM data is used for attitude determination, or in response to a flag in the spacecraft computer signaling a low power condition. Science Mode is the normal operating state. In this mode, the instrument payload is ready for full science data collection and is autonomously controlled by flight software using onboard triggers, as described in the Software Section of this paper. Finally, Engineering Mode enables safety critical operation. This mode can be entered by command only, typically during ground contact and in preparation for early operations (instrument health and safety diagnostics) and special case instrument operations (boom deploy and boom releases).

2.1 IDPU Core Electronics

2.1.1 Data Control Board (DCB)

The THEMIS DCB provides intelligence for the IDPU, controlling the flow of raw data through the memory system. It receives commands from the Probe's BAU processor and manages the instrument payload. A solid state recorder (SSR) is included on the DCB to eliminate a high bandwidth interface between the BAU and the IDPU, and to allow more control of the data recording by the IDPU. Science data volume drove the data storage requirement of 200 MB. The DCB formats data directly into packets and frames so it is ready for transmission without further processing. The processor is an 8085 microcontroller, running at 2.0 MHz. It is supported by an 8 K × 8 Boot ROM, SEU-Immune Static RAM, SSR SDRAM, and EEPROM. The 128 K × 8 SRAM is segmented and shared by the FPGA subsystems. The processing resources required for the IDPU are modest because the bulk of the high-speed data handling is done by the FPGA. Support circuitry in the FPGA includes address/data demultiplexing, memory decoding, and spacecraft interface logic. The DCB communicates with the instruments or their interface subsystems via dedicated serial command data interfaces (CDIs), receiving/storing data and forwarding instrument commands and register loads. An Analog to Digital Converter (ADC) on the DCB is used by the processor to collect analog housekeeping. Figure 2 shows an overview of the main subsystems comprising the DCB. The DCB resides on a 6U VME board, shared with the ETC (SST & ESA control subsystem). It connects to a backplane via a standard VME 96 pin connector. Power is received through the backplane connection, which is also used to communicate with the instrument support boards. A harness is used to connect the DCB to the Probe's BAU.
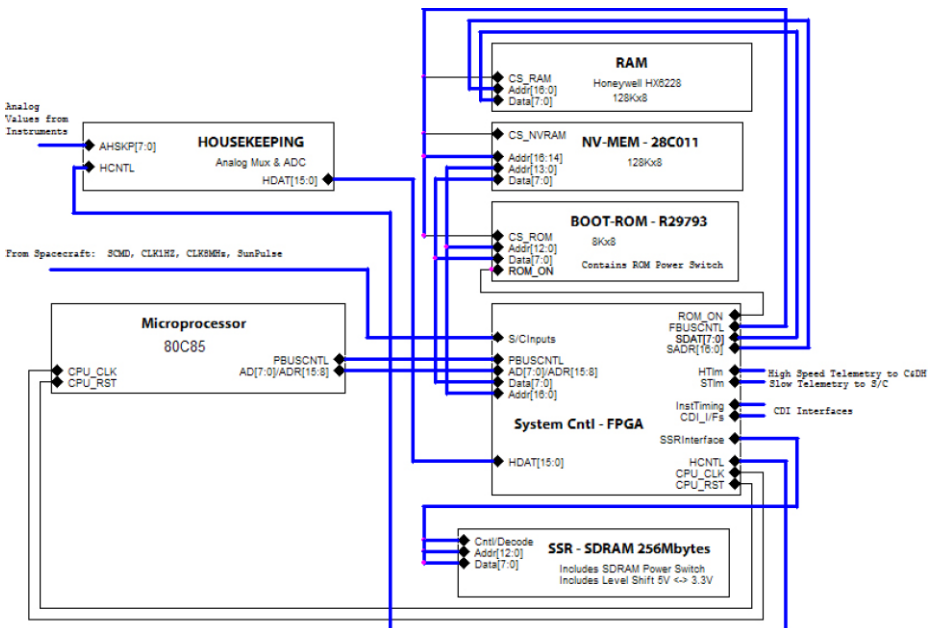

Fig. 2 THEMIS Data Control Board (DCB) block diagram

2.1.1.1 Processor   The DCB central processing unit (CPU) is an 8-bit radiation hardened processor 80C85RH with very low power requirements (< 100 mW). It provides control and monitoring of the instruments and data flow, collection of instrument housekeeping data, and is the sole interface between the instruments and the BAU. The processing function is shared by the DCB FPGA which handles the processor bus control and provides registers for accessing the various sections of memory. Included in the FPGA are the Instrument Interface Logic, the SDRAM controller, Error Detection and Correction (EDAC) for the SDRAM, the S/C Interface Logic, direct memory access (DMA) and data management control, analog housekeeping control, and timing/time-tagging support.

The IDPU has an overall reset capability, generated by the DCB FPGA. The reset is an OR of two sources: a power-on hardware reset (generated by an RC delay network and AC14 gate) and a watchdog reset. The watchdog reset pulse is generated if the CPU does not write to the Watchdog Reset Clear register for a period of 3 seconds. An external jumper allows the watchdog to be disabled during testing or debug. During test, a debug interface allows for the connection of external diagnostic peripherals and monitoring of the CPU Bus.

2.1.1.2 Memory   The CPU memory bus directly connects to the DCB FPGA and boot ROM (8 K × 8 Raytheon R29793). An external SRAM (Honeywell HX6228) resides on a private memory bus controlled by the FPGA and available to the CPU. An EEPROM (128 K × 8) provides non-volatile storage. A write-protect bit in the Control Register prevents spurious accesses. The EEPROM also contains internal write-protection mechanisms. The EEPROM resides on the CPU bus, and is not accessible to anything but the processor. At reset, EEPROM starts booting from address 0, where boot ROM is mapped. After boot-up, the CPU turns off power to the boot ROM via an on-board switch controlled by the FPGA, and executes directly out of RAM.

The address space of the processor (64 Kbytes) is much smaller than the total memory available. The processor accesses all the various memory locations by a combination of mapping and switching. When the ROM is off, the lower 32 K of address space is mapped to SRAM. The upper 32 K is switched between the remaining SRAM locations, EEPROM, and the SSR. Two page registers in the FPGA define the paging for the upper half (32 K) of CPU address space.

2.1.1.3 Spacecraft Interface   The IDPU-spacecraft (BAU) interface contains a 2 MHz High-Speed Telemetry Interface, a bidirectional UART operating at 38.4 Kbaud for Low Speed Telemetry and Commands, timing signals or Clocks, and a "Sun Pulse" signal from the BAU to the DCB. The UART signals are conditioned with differential RS-422 drivers/receivers. The transmission lines are shielded twisted pairs with the individual shield grounded at the driver end only.

Command Interface   The Command interface is a serial interface used to send data from the BAU to the IDPU. Data is transmitted at 38.4 Kbaud. Data is exchanged once per second and includes instrument specific commands, probe status information, and time. The probe status information includes instrument current draw, transponder status, maneuver status, eclipse flags, and thermal information.

Low Speed Telemetry Interface   The Low Speed Telemetry interface is a serial interface used to send housekeeping data from the IDPU to the BAU. The data is transmitted using UART encoding, and a differential interface. The UART is a standard 8-bit bidirectional UART operating at 38.4 Kbaud. Low-speed data is exchanged once per second and includes a housekeeping packet, containing instrument state of health data, and FGM data, used for attitude determination on the ground.

High Speed Telemetry Interface   The High Speed Telemetry (HST) interface is a bit serial interface used to transfer CCSDS-formatted instrument data telemetry packets from the SSR to the BAU for transmission to the ground. The HST interface transfers data in a single direction, from the IDPU to the BAU. Both the BAU and the IDPU must be enabled, by command, to participate in a transfer session. Packetization is in conformance with CCSDS Packet Telemetry recommendations, and includes primary and secondary headers followed by a stream of data. Data is transmitted to the high-speed link on a frame by frame basis. When the BAU is ready for a frame, it asserts a ready signal, at which point the DCB clocks out a bit-stream along with a clock synch corresponding to each data bit. The CPU is responsible for setting up the DMA transfer on a packet by packet basis. The FPGA inserts the variable sized CCSDS packets into fixed sized frames and generates the Transfer Frame Headers (both primary and secondary). The flow of data is not continuous; rather, it's broken into discrete transfers, or "Transfer Frames." The Transfer Frame has no Sync Word or Reed Solomon Block. These blocks are added to each frame in the BAU to produce the Master Frame, which is then ready for transmission to ground.

Timing   The IDPU receives Probe time in the form of two clock signals at 1 Hz and approximately 8.4 MHz plus a periodic synchronizing command. The Probe BAU has a stable, oven-controlled oscillator (OCXO) that provides timing for all the subsystems. The DCB internal time-base is set by a local oscillator at 20 MHz which is used by the FPGA as the overall system clock. The DCB generates a 1 Hz Clock directly from the Probe 1 Hz Sync when in "external clock mode" or via its own internal counter when in "internal clock mode." The time code is in UTC spacecraft time. The time value sent is 32 bits of integer seconds; the fractional seconds are zero at the time of the 1 Hz Clock pulse. This time interface is used to synchronize and time tag all instrument data, providing relative timing accuracy to 1 µs, and absolute time accuracy to about 1 ms.

Sun Pulse   A Sun Pulse is provided to the DCB once per spin, indicating the sun crossing. The Spin-Synch timing consists of a 14-bit counter, clocked by a programmable pulse generator. The upper 5 bits of the counter are used to generate the "SpinSector Pulse," while the full 14-bits are used to generate a "SpinSynch Pulse." Timing is supervised by the CPU, via a programmable pulse generator.

2.1.1.4 Instrument Interfaces   The processor communicates with the instrument support boards using a custom bi-directional serial Command and Data Interface (CDI) over the IDPU backplane. The backplane CDI is a serial protocol, synchronized to the 8.4 MHz clock provided by the spacecraft. Each subsystem receives its own set of CDI signals (Clock and Command) and returns message data via Telemetry signals. Each Clock is a continuous 2^{23} Hz signal (approximately 8.4 MHz) provided by the DCB in order to synchronize data transfers and to provide the basis of the common sampling clock. The CDI transfers data at 1 Mbps in 24-bit words, which include an 8-bit destination address and a 16-bit data value. No handshaking is required. The DCB is designed to ingest data as fast as the instrument boards can provide it. The instruments buffer commands as needed to keep up with several back-to-back commands.

2.1.1.5 Housekeeping   For Instrument housekeeping data, there is an analog-to-digital converter on the DCB board, along with an 8-input analog mux. The mux channel is selected via an ADC Control Register. Typically the CPU sets the mux channel to the next channel to be sampled, waits until the switch and low-pass filter have settled, and then starts

a conversion. In order to optimize for low-power, the ADC is kept in shutdown (nap mode, the default at reset) until the CPU is ready to perform a conversion. The inputs to the ADC come via the backplane. Each board has an analog housekeeping multiplexer attached to a common analog housekeeping signal on the backplane, which is routed to the ADC. The IDPU controls this distributed multiplexer tree via registers on the boards controlled over the backplane.

2.1.2 Power System

The IDPU power system was designed to be highly efficient ($>75\%$) while meeting the typical requirements of isolation, regulation, control and monitoring. The IDPU receives electrical power from the Probe on four separately switched services. Each service provides unregulated 28 V (28 ± 6 V). The primary BAU controlled 28 V service supplies twelve separate DC-DC converters containing both isolated and regulated outputs. A second BAU controlled 28 V service is used for actuator power and boom deployments. The third and fourth services are used for primary and secondary heater power respectively.

The primary IDPU converters are always powered and supply power to the IDPU and the instruments through individual switches. The Low Voltage Power Supply (LVPS) takes unregulated spacecraft 28 V power and generates the secondary voltages used by the IDPU and instruments. The normal power bus is regulated and converted into a number of secondary voltages, including $+5$ V and $+2.5$ V digital, ±5 V analog, ±8 V analog, ±10 V analog, ±12 V analog, $+28$ V regulated, $+4$ V analog, ±10 V floating, and ±100 V. Most of the secondaries are provided with approximately 0.5 V over-voltage so that they can run low-drop-out regulator/current limiters downstream on the boards. This provides clean power on the boards to reduce cross-talk, and also provides power isolation for fail-safe requirements.

Actuator power goes to the Power Control Board (PCB) where FET switches control its distribution to the boom mechanisms and motors. This service is switched on for boom deployments only and has the appropriate lock-out capability (through a separate enabling plug) required by safety during ground operations and launch vehicle processing.

Heater power is simply routed through the PCB to the instrument heater/thermostat circuits without conditioning. The heater services are switched on for all modes and controlled by Instrument thermostats.

Figure 3 shows an overview of the main components comprising the IDPU power system (LVPS and PCB). The Instrument payload enable switches are current limited and provide necessary isolation between the different instruments and the IDPU core subsystems. All other switches are simple FETs. The PCB incorporates a single FPGA that handles all power control functions and the CDI interface to the DCB. Analog housekeeping is multiplexed, addressed by commands to the PCB logic, and fed up the backplane to the DCB for A/D conversion.

2.1.2.1 Low Voltage Power Supply (LVPS)   The IDPU LVPS generates the various voltages required by the THEMIS instrument suite from the unregulated 28 V Probe power. Regulated voltages are Pulse Width Modulated (PWM) and regulated to $\pm1\%$. Voltages regulated by similarity are regulated to $\pm5\%$. The output ripples were designed and tested to be less than ±10 mV rms. The current monitor ranges are 2.5 V full scale for each monitored voltage. Each power supply is current limited on its primary side and is galvanically isolated primary to secondary. The input from the 28 V Probe power is soft started and filtered to meet EMI requirements.

Fig. 3 LVPS/PCB block diagram

Distributed IDPU Voltages   The LVPS was required to provide analog voltages (±5 VA, ±8 VA, ±10 VA) and digital voltages (+2.5 VD, +5 VD) for distribution on the backplane to the other IDPU boards. The input current for each service is monitored and reported to the DCB. All voltages appear with the presence of 28 V Probe power and are then separately switched on the PCB for distribution to the instruments. Positive and negative headroom voltages (±12 VA) are also provided to operate current monitors and limiters on the PCB. The +2.5 VD, +5 VD, and +5 V are regulated; the other voltages regulated by similarity. The presence of the +2.5 VD supersedes the presence of the +5 VD for FPGA power. The sequencing is in compliance with the FPGA requirements as specified by the manufacturer.

Regulated 28 V *ESA Voltage*   The LVPS provides a separate converter for regulated 28 V that is used to power the ESA electronics and detector high voltage supplies. The high voltage supplies provide a programmable output up to 5000 V.

SMA Voltage   The LVPS provides a regulated 4 V used to power actuators resident in many of the THEMIS mechanisms. The actuators are Shape Memory Alloy (SMA) systems, which provide a force when heated by passing current through them. The SMA voltage is switched on at command from the DCB.

EFI Floating Voltages   The LVPS provides each axis (X, Y, Z) of the EFI instrument with pairs of ±10 V, and each set a separate "floating" return. A separate line from the DCB commands each pair. The voltages are derived from a regulated +5 V and their regulation are proportional to it.

EFI Voltages   The LVPS provides ±5 VA, ±10 VA, +2.5 VD, and +5 VD to be used by the fields experiment BEB and DFB. The input current is monitored and reported to the DCB. The voltages are enabled by a command from the DCB. The +5 V, +5 VD and

the 2.5 VD are regulated; the other voltages regulated by similarity. The presence of the +2.5 VD supersedes the presence of the +5 VD for the DFB FPGA.

The LVPS resides on a 6U shielded and pocketed board. It connects to the rest of the IDPU via a Hypertronics connector. Power is received from the Probe BAU through a standard, redundant 9-pin connector.

2.1.2.2 Power Control Board (PCB) Following the LVPS DC-DC converters is a power controller switch bank on the PCB which consists of 45 switches, controlled by 28 logic signals (one for each instrument or actuator). Switched power services resident on the PCB include: instrument control (9); operational heater power switching (5); and actuator power switches for the instrument actuators (SST attenuators (2), ESA cover (1), EFI doors (4), SCM and FGM booms and back-up (4), and EFI Axial Boom (AXB) and back-up (3)). The current limiters latch (exceeding the current limit will interrupt the service until it is reset by the DCB) to limit power dissipation in the transistors. Both current and voltage are monitored on all voltage services and these values are read by the processor via the DCB housekeeping system, and stored for instrument health and safety.

The PCB resides on a 6U VME board, shared with the FGE. It connects to the backplane via a standard VME 96 pin connector. Power is received and distributed through the backplane connection. Actuator and heater power is received from the Probe BAU through separate standard connectors.

2.2 IDPU Instrument Support Electronics

In addition to the core instrument electronics, the IDPU houses the instrument specific electronics which consists of the boards as described below.

The BEB and DFB support the fields experiment and share one switched power service. Their CDI Interface is also shared. The BEB does not output messages, but uses the CDI for command reception. The DFB connects directly to the analog outputs of the EFI and SCM sensors, performs processing and programmable filtering (see Cully et al. 2008). The Boom Electronics Board (BEB) contains power supplies and DACs to control the EFI sensors bias settings (see Bonnell et al. 2008).

The FluxGate Magnetometer Electronics (FGE) controller for the FGM connects to the FGM sensor via an external harness, processes data and generates messages. (FGE shares a board with the PCB, but each subsystem has its own CDI since the FGE power service is switched) (see Auster et al. 2008).

The ETC Subsystem shares a board with the DCB, but communicates with the DCB using an interface similar to the other IDPU subsystems. The ETC receives commands and timing signals, and generates messages from the particles experiment. The ETC subsystem controls the ESAs (Electrostatic Analyzers) and SST-DAP board. It acts as a router during data collection and generates trigger inputs such as moments (see Larson et al. 2008).

The Solid State Telescope Analog-to-Digital Processing Board (DAP) houses the SST LookUp tables, accumulation RAM and ADCs. The DAP receives commands and timing signals from the DCB and returns telemetry, which is processed by the ETC (see Larson et al. 2008).

3 Software Description

The THEMIS IDPU Flight Software (FSW) is responsible for instrument power control, time and attitude determination, mass memory control, science instrument control, command distribution, telemetry formatting and boom deployments. The flight code follows a

Fig. 4 FSW module connections

CSC#	Function	Name	Segment
1	Executive	EXEC	PROM
2	Background	BKG	PROM
3	Commands	CMD	PROM
4	Telemetry	TM	PROM
5	Housekeeping	HSK	PROM
6	Loader	LD	PROM
7	Utilities	UTIL	PROM
8	Input/Output	IO	PROM
9	Power Manager	PWR	PROM
10	SSR Manager	SSR	PROM
11	ACS	ACS	PROM
12	EFI Manager	EFI	PROM
13	ETC Manager	ETC	PROM
14	FGM Manager	FGM	PROM
15	SCM Manager	SCM	PROM
16	EFI Deployment	DEP	PROM
17	EFI/FGM Fit Manager	FIT	EEPROM
18	Spin Fit Calculator	SPIN	EEPROM
19	Matrix Solver	MATRIX	EEPROM
20	Trigonometrics	TRIG	EEPROM
21	Fast Floating Point	FFP	EEPROM
22	Compression Algs	CMP	EEPROM
23	Science Optimization	SCI	EEPROM
24	Software Changes	EEP	EEPROM

long line of software products now flying on a number of spacecraft, most closely resembling the Fast Auroral Snapshot (FAST) IDPU (see Harvey et al. 2001).

The THEMIS software is comprised of the 24 modules, totaling just over 19250 lines of assembly code. It requires 16.8 Kbytes of code space and 14 Kbytes of RAM. The FSW was developed in four phases, basically paralleling the instrument electronics development.

The 24 software modules can be functionally grouped into four main elements, as seen in Fig. 4 and described by module in more detail below. Modules 1–8 provide the core processor functions. Modules 9–15 interface to other instrument cards in the IDPU and control instrument sensors. Modules 16–21 are data analyzers and one-time use, and Modules 22–24 are optimizers. Figure 5 shows how the modules are connected and the information that passes between them.

The IDPU software splits the workload into Foreground (EXEC) and Background (BKG). The Executive runs the long-term tasks, anything requiring more than 2 milliseconds to perform. The BKG module splits a 256 Hz interrupt into a number of low-frequency interrupts for modules depending upon their requirements. The Command (CMD) module decodes, checks and distributes commands to other modules within the program. The Loader (LD) module provides loading and dumping capabilities. The Housekeeping (HSK) module samples all the A/D values for internal use and for use by the Telemetry (TM) module in generating telemetry. The TM module formats low speed and high speed telemetry. The Utility
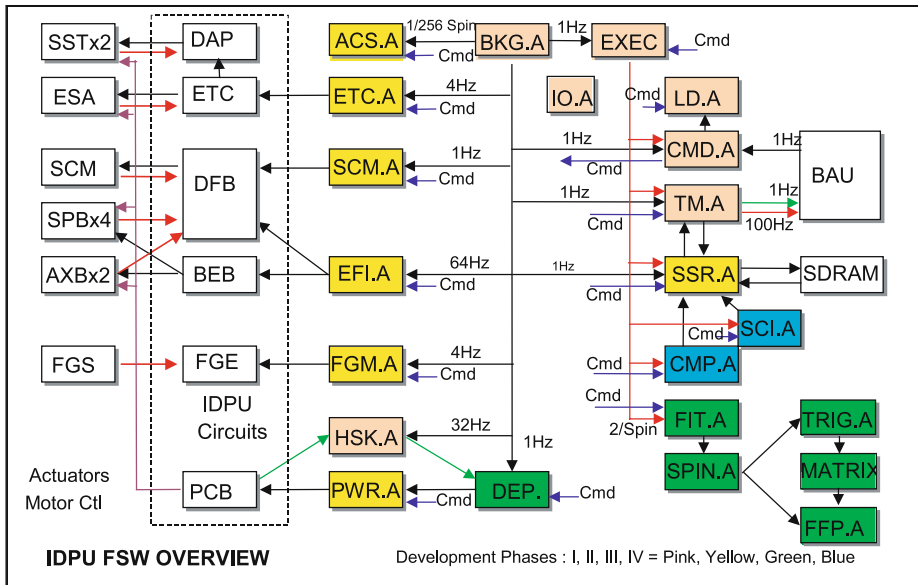
Fig. 5 FSW module connections

(UTIL) module provides common utilities for all the modules and the IO module provides device independence.

The Power Manager (PWR) controls to the instruments. The SSR module stores and retrieves data from the 200 MB memory. The ACS module provides a phase-locked-loop control of the Spin Sectoring for the sake of the ESA and SST instruments. Device drivers include the EFI, ETC, FGM, and SCM modules which communicate with their respective instrument electronics. And, the Deployment (DEP) module deploys the EFI Spin Plane Booms in a balanced fashion.

The next 5 modules are data analyzers, performing the necessary mathematical computations on the data.

The last three modules; CMP, the SCI, and the EEP modules provide data compression, burst data collection optimization and a host of small change requests, respectively.

3.1 Core Processor Functions

Executive (EXEC)   The EXEC module is responsible for system initialization, mode implementation and foreground coordination. Specifically, it handles ROM Execution, EEP-ROM Selection and Execution. For radiation tolerance, a bootstrap version of the flight code is stored in ROM and later versions are kept in an EEPROM. Whenever the IDPU is powered on, the ROM is mapped to the start of the memory address space, and the flight software operates briefly from the ROM. Upon initialization, the ROM immediately copies itself to a specific segment of RAM and then, through a hardware select circuit, swaps the RAM into low memory. The ROM is then powered off, leaving the bootstrap version of the flight program running in RAM. This process takes only a few milliseconds. For the first ten seconds, the IDPU runs the bootstrap program. This program initializes all the internal program modules, sets default values, and begins communicating with the Probe BAU immediately. During this time, the IDPU adopts a minimum power level, with only the core

systems (DCB, LVPS and PCB) powered on, and all the instruments powered off. Unless commanded to stop within the first ten seconds, the FSW checks over the four available EEPROM programs and automatically loads and executes the latest flight software version. Thus, the flight code runs entirely in RAM, requires no ROM or EEPROM power, and is directly patchable by ground command.

Background (BKG)   The BKG module is the timing coordinator for the IDPU software. Its job is to service and distribute the interrupts of the processor so that the system is responsive to physical events. Thus, the other modules are isolated from the details of the CPU interrupt hardware, and the background manager is able to level the load. The background module uses the clock interrupt to receive and maintain Universal Time (UT) and to ensure that all time stamps have the correct time. During each second, the IDPU software receives 256 interrupts per second based upon the spacecraft-provided 2^{23} Hz clock. Using these interrupts, the Time register is maintained to 1/256ths of a second. For packets requiring the most precise time possible, the input clock register may be read by FSW and stamped on each packet header.

Command (CMD)   The CMD module is the process by which all commands enter the IDPU. It sets up the DMA transfers, receives the packets, decodes them and distributes commands to appropriate modules. For command and control functions, the IDPU communicates with the BAU using a low rate serial line. Once per second the spacecraft and instrument exchange fixed-length blocks of data over this serial interface. This instrument side of the serial interface is connected to the processor via Direct Memory Access (DMA). The DMA transfers the data directly from/to processor memory. There are several types of command blocks executed by the FSW, each identified by their Application ID and Function Code.

Telemetry (TM)   The TM module is the process by which all telemetry is generated by the IDPU. It sets up the DMA transfers. The TM module is the central coordinator of telemetry generation and playback. Once per second, the TM module collects and formats IDPU engineering data, both digital and analog status, into an SOH packet. Double-buffering is used to put a new SOH packet into one buffer while the previous data is being transmitted.

Housekeeping (HSK)   The HSK module is responsible for collecting A/D samples for the flight software. Using a 32 Hz interrupt time, the HSK cycles through a list of multiplexer addresses and collects the data. Both 8-bit and 16-bit data are collected in separate lists for convenience. The ordering of the samples is defined by a PROM table which calls out the subsystem and the multiplexer within that subsystem.

Loader (LD)   The LD module is responsible for loading (patching) SRAM and EEPROM from the ground, as well as dumping blocks of data to housekeeping.

Utility (UTIL)   The UTIL module is a collection of general purpose routines which extend the capabilities of the 8085 processor. This module provides support functions for the flight software including memory clearing and copying, bit manipulation, 16-bit math and array functions.

Input/Output (IO)   The IO module is the logical-to-physical separation layer of the software.

3.2 Instrument Control Functions

Power (PWR) Manager   The PWR module provides power supply and actuator control under both direct ground command and internal calls from software modules. The module controls the LVPS and PCB, the latter through the use of the CDI. This module controls a number of one-time actuators, plus the SST attenuator multi-use actuators. The PWR module controls one actuator at a time and rejects other requests for activation while another activation sequence is in progress. It verifies that the selected actuator is enabled before allowing it to be fired. If not enabled, the FIRE command will result in an error message and no actuation takes place.

Solid State Recorder (SSR) Manager   The SSR module is responsible for the maintenance of the SSR system, including error scrubbing, memory segmentation, and memory pointer management. The SSR module turns on SDRAM power and defines an initial memory configuration, as well as the minimum number of packets needed in a segment to allow transmission. The SSR module uses the SDRAM exclusively for variable length CCSDS packets ranging from 1 to 4 KB in length. In order to make the transmission of these data easier, the header and data sections of these packets are contiguous in memory, and all packets begin on a 4 KB boundary. The SDRAM is divided among a number of storage areas, each managed by separate logic in the SSR module. The SSR module can be commanded to reconfigure memory with different allocations of Engineering, Quick Look, Survey, Particle Burst and Wave Burst data.

The ECC scrubber in the SSR module is hardwired to operate on the lower 200 MBytes of SDRAM. (The upper quarter of SDRAM is reserved for the check bits). Single Bit errors are automatically corrected and counted. Multiple-bit errors are counted. The two counters (Single Bit and Multiple Bit Errors) are read and reset via the FPGA Register Interface. Each counter is allocated 8-bits, telemetered in housekeeping, and can be cleared by the CPU. The upper bits of scrubber current addresses are also available as status so that CPU can monitor the error counts periodically, and determine if SDRAM failures are address dependent.

Attitude Control System (ACS)   The ACS module is responsible for the spin period and spin phase control of the instrumentation. It is responsible for determining precision spin information using the sun pulse signal from the spacecraft and an accurate clock. ACS software controls the DCB spin sectoring circuit which provides 2^{16}, 2^5 and 2^0 pulses per spin. Each timing register is 16-bits of subsecond time information. The FSW must properly apply UT to generate the correct time of these events. The ACS module is also able to read the current spin phase to 8-bit resolution for use in fine-tuning the spin synchronization.

Instrument Managers (EFI, ETC, FGM, SCM)   After reset, the Instrument manager modules set up the initial configuration of the DMA channels, set the I/O configuration for DMA swaps, and generate default telemetry headers for each instrument (EFI, ETC, FGM and SCM). The modules do not send commands at this time, since all instrument circuits are turned off by reset. The modules process commands in 2 ms or less, per the system requirement. For CDI lists, the modules start a command list processor going which uses subsequent interrupts to execute commands in the list until all are exhausted.

The EFI module manages the DFB and BEB interfaces for commands and telemetry. The ETC Module is responsible for controlling the ETC circuit, the DAP board, the SST sensor and the ESA sensor. In addition to housekeeping functions, this module controls the ESA HV registers, stepping the HV up to a target position at a programmed rate. The FGM

module is responsible for the FGE circuit and the FGS sensor. The SCM module manages the SCM instrument interface for calibration and engineering status (filter banks). To ensure the instrument does not stay in calibration mode, the SCM module uses an 8-bit maximum value for the calibration mode timer and counts at 1 Hz or greater to guarantee that the signal is turned off in less than 256 seconds. The SCM module does not need to direct SCM science measurements to the SSR since this function is handled by the DFB board under the control of the EFI module.

EFI Deployment   The DEP module is responsible for deploying the EFI Spin Plane Boom (SPB) units. Deployment of the spin plane booms systems is normally performed in pairs by the DEP module. The operator selects which pair of booms to deploy, and then gives the deployment length. The rest is automatic. If need be, deployment of one boom at a time can be performed by either using the DEP commands or direct CDI Motor control commands. Each boom unit is equipped with a turns-counter microswitch which is sampled by the IDPU software to track the length deployed. Since the booms deploy at slightly different rates, software monitors the lengths and if one boom gets more than 2 'clicks' ahead of the opposite boom, the longer boom is paused until the shorter boom catches up.

3.3 Data Analyzers

EFI/FGM Fit Manager (FIT)   The FIT module is responsible for collecting samples from the EFI spin plane boom and FGM instruments, and performing Sine-Wave Least Squares Fits of these data. Each fit provides the Electric Field and Magnetic Field vectors in the spin plane along with the averaged Z-axis component and standard deviation of the fit. The result is in 4 floating point scalars, A, B, C and Sigma where the vector is the waveform is $A + B\cos(\omega t_i) + C\sin(\omega t_i)$. The terms of the fit are shown in Fig. 6 and the matrix shown in Fig. 7. Each fit requires approximately 0.4 seconds.

Spin Fit Calculator (SPIN)   The SPIN module is the calculator of the Sine-Wave-Least-Squares fit function. The Spin Fit calculator uses this function to determine the Electric Field and Magnetic Field strength and direction.

$$F = \sum_{i=1}^{N} [E(t_i) - (A + B\cos(\omega t_i) + C\sin(\omega t_i))]^2$$

$$\frac{\Delta F}{\Delta A} = \sum_{i=1}^{N} -2[E(t_i) - (A + B\cos(\omega t_i) + C\sin(\omega t_i))]$$

$$\frac{\Delta F}{\Delta B} = \sum_{i=1}^{N} -2[E(t_i) - (A + B\cos(\omega t_i) + C\sin(\omega t_i))] - \sin(\omega t_i)$$

$$\frac{\Delta F}{\Delta C} = \sum_{i=1}^{N} -2[E(t_i) - (A + B\cos(\omega t_i) + C\sin(\omega t_i))]\cos(\omega t_i)$$

$$\Gamma = \sqrt{F/(N-1)}$$

Fig. 6 Spin fit formulae

Fig. 7 Spin fit matrix

A	B	C	
N	$\sum_{i=1}^{N} \cos$	$\sum_{i=1}^{N} \sin$	$\sum_{i=1}^{N} E(t_i)$
$\sum_{i=1}^{N} \cos$	$\sum_{i=1}^{N} \cos^2$	$\sum_{i=1}^{N} \sin\cos$	$\sum_{i=1}^{N} E(t_i)\cos$
$\sum_{i=1}^{N} \sin$	$\sum_{i=1}^{N} \sin\cos$	$\sum_{i=1}^{N} \sin^2$	$\sum_{i=1}^{N} E(t_i)\sin$

Matrix Solver (MATRIX)   The MATRIX module is a general 2×3 or 3×4 matrix solver using a Fast Floating Point format. It uses a standard process of diagonalization, and uses a practical zero of 10E–40.

Fast Floating Point (FFP)   The FFP module is a collection of Fast Floating Point routines developed by Dave Curtis and Peter Harvey in 1980 and flown on numerous UCB spaceflight instruments for the last 24 years. The source code and description was written by UCB for the AMPTE and CRRES projects. The FFP module is used for on-orbit data analysis (sine wave least squares fit subroutine with sufficient range and precision of floating point) of the DC electric and magnetic fields.

3.4 Optimizers

Compression Algorithms (CMP)   The CMP module is responsible for the compression of science and engineering data in the SSR. The CMP software requests packets from the SSR, compresses each packet based on the APID, and marks it as compressed. For the vast majority of the time, the survey packets are compressed right after they are stored in the SSR. When all the survey is compressed, completed Burst segments are compressed (highest value first).

The CMP module runs at a variable rate through the memory since the compression rate is dependent upon the specific data set. Typically, compression runs around 100 Kbps. Compression is enabled to operate on a given segment of memory which is not simultaneously enabled for telemeter to ground. The CMP module comes up disabled and will not disturb memory unless enabled to do so. The CMP module operates in the Executive level of the processor, but does not have to meet interrupt timing requirements.

For a given packet, the CMP module decodes the APID and references an APID-to-Algorithm list to determine the proper compression algorithm to use for that data. Generally speaking, Huffman works best on counter data (ESA/SST) and DeltaMod works best on Field data (EFI, FGM, SCM).

Science Optimization (SCI)   The SCI module is responsible for the science level operation of the Instrument. If information is shared between two instruments, or the operation of one instrument is virtually controlled on the outputs of another instrument, the science module is responsible for making this inter-instrument connectivity. It provides the optimum configuration of the electronics and sensors to return the best science data.

Most importantly, the SCI module samples science and engineering data in order to trigger on significant events and saves that data in the SSR. The IDPU electronics provides a

number of data sets which are considered useful for triggering, including: ESA and SST ion and electron full distribution and reduced distribution data sets; EFI DFB Filter-Bank outputs; and magnetic field spin fit data. The trigger data is used to change instrument modes from survey (Slow or Fast) to burst (particle or wave). Particle Bursts are slow processes and the data is gathered in a matter of spin periods. Wave Burst phenomena are quick and the data must be collected and evaluated quickly, e.g. several times per second.

In addition to trigger functions, the SCI module averages the voltage inputs from the EFI sensors and produces the spacecraft potential each spin. This value is made available for the ETC module to send to the ETC chip in order to adjust its accumulations.

Software Changes (EEP)   The EEPROM module provides a collection of software changes to the boot software. As the first module of the EEPROM memory, this software is executed after the EEPROM code is loaded and is therefore responsible for installing patches for the EEPROM module and calling the initialization routine for SCI module. Patching the ROM area is possible since the ROM area of memory is copied to RAM and electronically swapped into the memory map at address 0. Thus, by the time that the EEPROM is executed (at reset plus 10 seconds), the EEPROM can simply modify the ROM area at will.

4 Conclusion

The THEMIS probes required a sophisticated, central Instrument Data Processing Unit (IDPU) to operate the large instrument suite and to collect the high resolution data necessary for the scientific objectives. The IDPU routes commands to the various instrument support boards, controls the power system, collects instrument housekeeping, controls boom deployments, directs science data to the mass memory, and optimizes the data downlinked to the ground by prioritizing data selection and incorporating triggering algorithms. A design philosophy was employed that provides autonomous instrument data accumulation rate control with minimal commanding and a data recording system with minimal processor interaction. Custom designed FPGAs perform numerous tasks normally delegated to a processor. With a reduced work load for the processor, the software focuses on data optimization and compression schemes that maximize the science return. The simple, flexible design of the THEMIS IDPU has been essential to the success of the mission. The hardware and software design description discussed here can be used to help integrate multiple instruments into a single experiment on future constellation missions that are typically mass and power constrained.

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