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INTRODUCTION

See "ISUAL Functional Specification", UCB SSL Drawing No. 8445-W7, for general requirements of the ISUAL Mass Memory.

The ISUAL Mass Memory (MM) is a large memory for storing raw and compressed science data for the ISUAL instrument. The MM exists as a module in the Auxiliary Electronics Package (AEP), the main collection of electronic controls for the ISUAL instrument. The MM module includes:

- Semiconductor memory devices
- Interfaces to other AEP modules
- Memory request priority circuits
- Memory address and data buffer circuits
- Error detection and correction circuits (TBD)

FUNCTIONAL

The MM holds one gigabit of data in volatile memory devices. It receives data from the Spectrophotometer, Array Photometer, and CCD Imager. It sends data to the ROCSAT2 spacecraft via a serial telemetry interface. It is accessible for reading and writing by the CIC (DSP) and DPU modules of the AEP.

MECHANICAL

The MM is packaged as a printed circuit board in an aluminum frame and is located between the DPU and CIC modules in the AEP.

ELECTRICAL

The MM is powered from the Power Controller (PC) module, and its power services are under control of the DPU module. The DPU can turn the MM power on and off independently of other modules. The DPU can operate with the MM power on or off.

THERMAL

Heat generated by circuits in the MM module is dissipated by conduction through the printed circuit board to the frame and from the frame to TBD. One thermistor in the MM is wired to the housekeeping circuits on the DPU.

ENVIRONMENTAL

TBD

INTERNAL ORGANIZATION

The one-gigabit MM memory is organized as 128 kilobytes of eight bits each. The memory may be accessed by (TBD) byte, word (16 bits), or double word (32 bits).

INTERFACES

Seven interfaces connect the MM to other parts of the ISUAL instrument:

- CCD Imager
- DSP
- DPU
- Array Photometer (AP)
- Spectrophotometer (SP)
- Telemetry
- Power

Each interface is designed specifically for the needs of the subsystem and its data rate.

CCD Interface

When the CCD is capturing an image, it sends data to the CIC at a high rate, and the CIC forwards this data to the MM. The MM receives the data and stores it via a DMA mechanism at incrementing addresses. The starting address and buffer size are controlled by the DSP or DPU (TBD).

A 12-bit (or 24-bit, TBD) parallel interface with handshaking signals carries the CCD data from the CIC to the MM via the BUS connector.

- One pixel each 125 nanoseconds
- 12 bits/pixel
- Bandwidth needed = 96 Mb/s
- Data width TBD
- Write only
- Sequential access
- High priority

DSP Interface

The DSP (on the CIC) has direct read/write access to the entire MM via the DSP's address and data buses. During the collection of data by the CCD imager, the DSP may perform an occasional access of the MM and may be held off briefly by a wait signal if another MM interface is completing a memory cycle. During non-collection periods, the DSP will have frequent and primary access to the MM for processing and compressing raw CCD data. In addition the DSP and DPU will exchange command and status information via short blocks in the MM.

A parallel interface with 16 data lines, 26 address lines, and a few control lines connects the DSP to the MM via the BUS connector.

- 16 bits per memory access (or DSP data bus width, TBD)
- 100 ns (TBD) per DSP memory cycle
- Bandwidth needed = TBD Mb/s
- Read/write
- Random access

- High priority

DPU Interface

The DPU has read/write access to the entire MM via the DPU's address and data buses. Since the MM address space is much larger than the DPU's addressing range, a bank switching scheme will convert DPU addresses to MM addresses. A bank will likely be 16 kilobytes, and the bank switching will likely be an extension of the IMAGE memory bank structure. The DPU's primary access to the MM will be for the exchange of command/data blocks with the DSP.

A parallel interface with 8 data lines, 14 address lines, and a few control lines connects the DPU to the MM via the BUS connector.

- One byte per memory access
- 1524 ns per DPU memory cycle
- Few hundred bytes/s (TBD)
- Bandwidth needed = 4 kb/s (TBD)
- Read/write
- Random access
- Low priority

Array Photometer Interface

The Array Photometer (AP) sends a continuous stream of samples to the MM, and the MM stores them in a circular buffer via DMA with an auto-incrementing address. The size and location of the buffer are set up by the DPU.

A three-wire serial interface (data, clock, strobe) carries AP data from the API to the MM via the BUS connector.

- 2 x 16 x 10 kHz sample rate
- 12 bits/sample
- Bandwidth needed = 3.84 Mb/s
- Write only
- Sequential access
- Medium priority

Spectrophotometer Interface

The Spectrophotometer (SP) sends a continuous stream of samples to the MM, and the MM stores them in a circular buffer via DMA with an auto-incrementing address. The size and location of the buffer are set up by the DPU.

A three-wire serial interface (data, clock, strobe) carries SP data from the SPI to the MM via the BUS connector.

- 6 x 10 kHz sample rate
- 12 bits/sample
- Bandwidth needed = 720 kb/s
- Write only
- Sequential access
- Medium priority

Telemetry Interface

The DPU sends science and housekeeping data to the spacecraft telemetry buffer. The DPU supplies a few header and trailer bytes for each packet, but the data portion comes from a block in the MM. The DPU sets up the size and location of this block, then the MM supplies the contents via DMA with an auto-incrementing address. (DPU hardware receives the data from the MM, then forwards it to the spacecraft telemetry buffer.)

A three-wire serial interface (data, clock, CTS) will carry the telemetry data from the MM to the DPU.

- 1106 bytes/packet
- Bandwidth needed = 2 Mb/s
- Read only
- Sequential address
- High priority

Power Interface

Power services from Power Controller to MM, controlled by DPU, as follows:

+5 volts at TBD mA
+12 volts at TBD mA
-12 volts at TBD mA
TBD watts nominal

BANDWIDTH

If all interfaces operate at their maximum rates, the following approximate instantaneous memory bandwidth would be required:

CCD 96 Mb/s
DSP (TBD)
DPU 4 kb/s
AP 3.84 Mb/s
SP 720 kb/s
TLM 2 Mb/s

Total 102.6 Mb/s + DSP

This total bandwidth may exceed the final design bandwidth of the MM. However, no interface is precluded from operating simultaneously with any other, except as limited by total memory bandwidth.