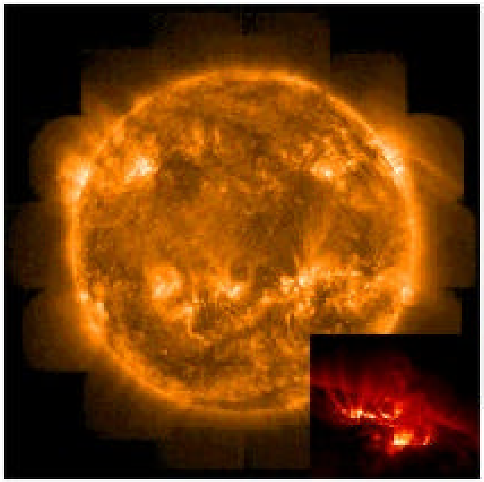
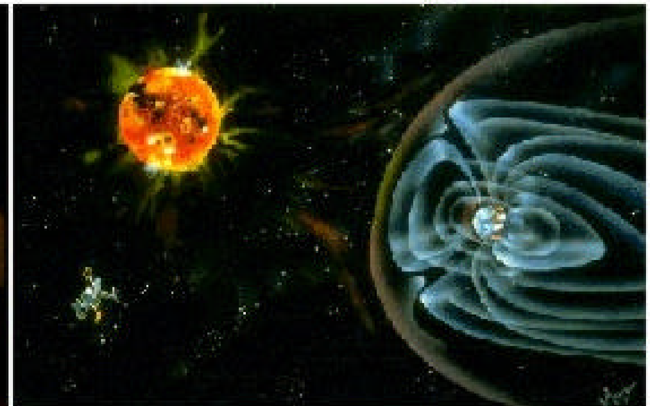




IMPACT
measures the invisible particles and fields that reach across interplanetary space from the Sun to affect the Earth

Volume 2

Agenda

11 Sept.		
09:00	Introduction, Science Overview	Luhmann
09:45	IMPACT Project Overview	Curtis
10:00	IMPACT System Engineering	Curtis
11:00	Reliability	Sanford
11:15	MAG	Acuna
12:00	Lunch	
13:00	Boom (Mechanical, Thermal)	Ullrich
14:00	SWEA	Cotin
15:00	STE	Curtis
16:00	IDPU / LVPS	Curtis
17:00	EGSE	Curtis
17:30	Suite Integration and Test	Curtis
12 Sept.		
09:00	SEP Overview	Tycho
10:00	SEPT	Tycho
11:00	HET	Tycho
12:00	Lunch	
13:00	LET, LET/HET Detector Status	Wiedenbeck
14:00	SEP Central Electronics (&LET electronics)	Cook
15:00	SIT	Mason
16:00	SEP Mechanical & FOV	Tycho
16:45	SEP Thermal	Hawk
17:00	SEP I&T	Tycho
17:30	SEP Issues and Concerns	Tycho
17:45	Mission Operations & Data Analysis plans	Curtis
18:00	Action Item Review	

STEREO IMPACT/SEP OVERVIEW

Tycho von Rosenvinge

Solar Energetic Particles
Preliminary Design Review
2001-September-12, APL

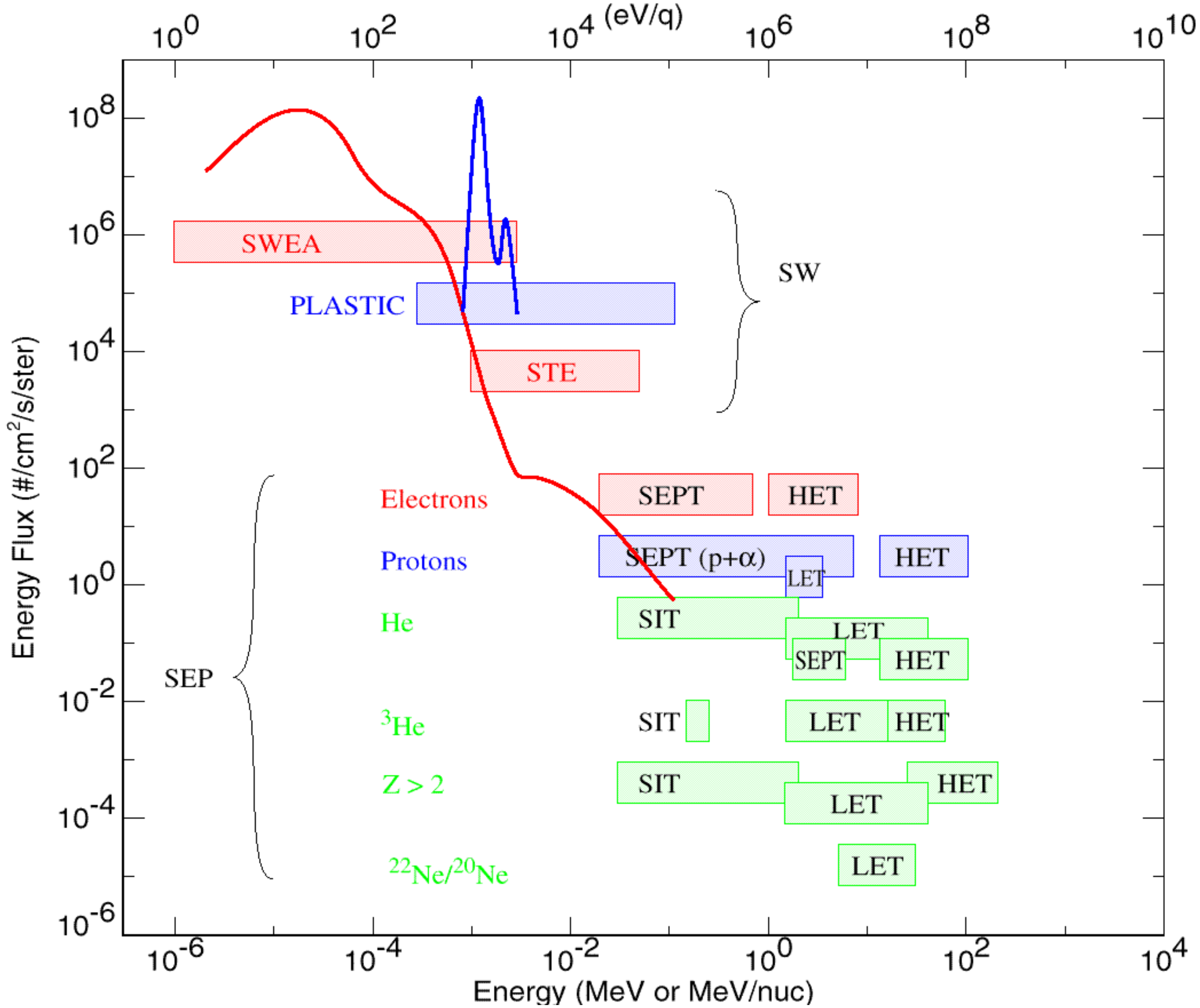
IMPACT Science Summary

Table A.1 IMPACT Summary

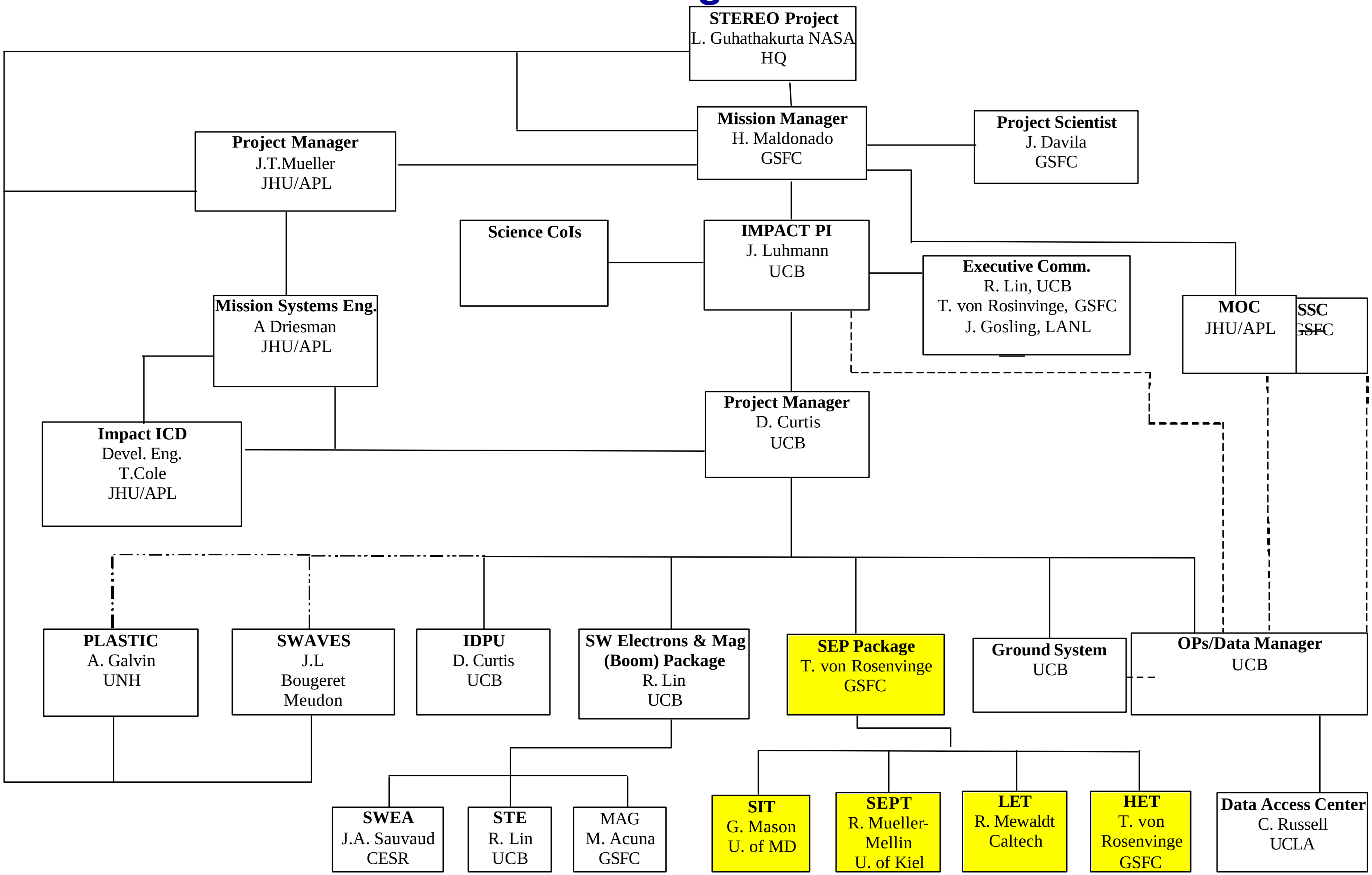
Experiment	Instrument	Measurement	Energy or Mag. field range	Mass (kg)	Power (w)	Data Rate (bps)	Time Res.	Instrument provider
SW	STE	Electron flux and anistropy	2-100 keV	0.35	0.20	64	16 s	UCB (Lin)
	SWEA	3D electron distrib., core & halo density, temp. & anisotropy	~0-3 keV	1.71	1.10	394	3D=1 min 2D=8s Mom.=2s	CESR (Sauvaud) + UCB (Lin)
MAG	MAG	Vector field	±500nT, ±65536 nT	0.25	0.0	154	1/8 s	GSFC (Acuna)
SEP	SIT	He to Fe ions	0.03-2 MeV/nuc	0.93	0.66	240	30 s	U. of Md. (Mason) + MPAE (Korth) +UCB (Curtis)
		^{3}He	0.15-0.25 MeV/nuc				30 s	
	SEPT	Diff. electron flux	20-400 keV	1.06	1.04	120	1 min	U. of Kiel (Mueller-Mellin) + ESTEC (Sanderson)
		Diff. proton flux	20-7000 keV				1 min	
		Anistropies of e,p	As above				15 min	
	LET	Ion mass 2-28 & anisotropy	1.5-40 MeV/nuc	0.51	0.18	320	1-15 min.	GSFC (von Rosenvinge) + Caltech (Mewaldt) + JPL (Wiedenbeck)
		^{3}He ions flux & anistropy	1.5-1.6 MeV/nuc				15 min.	
		H ions flux & anistropy	1.5-3.5 MeV				1-15 min.	
	HET	Electron flux	1-8 MeV	0.70	0.07	120	1-15 min.	Caltech (Mewaldt) + GSFC (von Rosenvinge) + JPL (Wiedenbeck)
		H	13-100 MeV				1-15 min.	
		He	13-100 MeV				1-15 min.	
		^{3}He	15-60 MeV/nuc				15 min	
	SEP Common	----	----	1.69	1.55	----	----	Caltech (Mewaldt) + GSFC (von Rosenvinge)
IMPACT Common	IDPU (+Mag Analog)	----	----	1.73	3.60	164 +524 Burst	----	UCB (Curtis)

IMPACT is a suite of 7 instruments built at 9 institutions by 31 Co-Investigators**.**

IMPACT / PLASTIC Energy Coverage



IMPACT Team Organization Chart



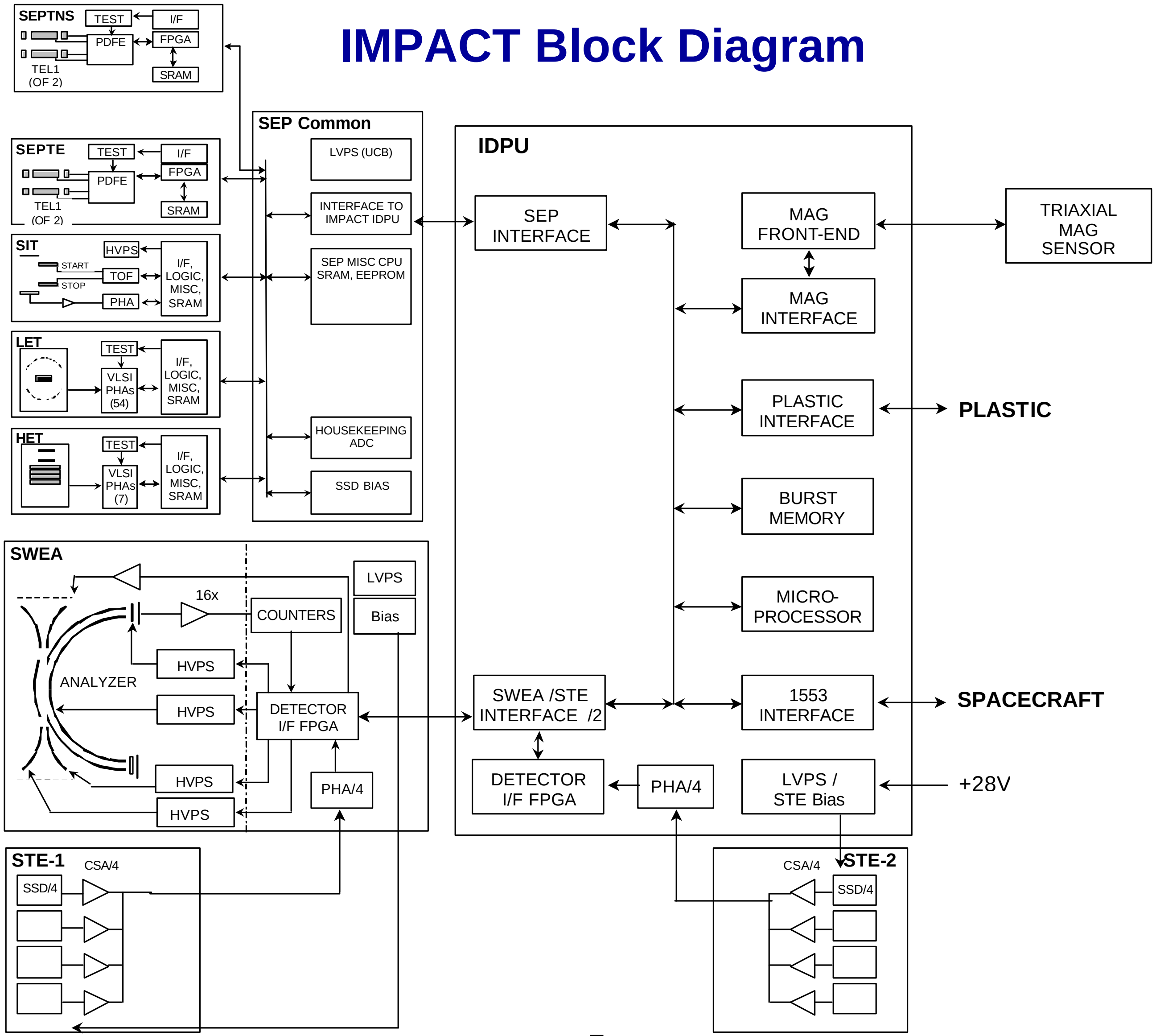
SEP Responsibilities

- University of Kiel
  - Design/fabrication/test of SEPT telescopes
- ESTeC
  - Design/fabrication/test of SEPT Electronics
- U of MD
  - Overall responsibility for design/test of SIT
- Max Planck/Lindau
  - Digital portion of SIT Time-of-Flight system
- Caltech
  - Low Energy Telescope development/test
  - Common SEP electronics, ASIC development, central data processing unit, Low Energy Telescopes
  - Overall integration/test of SEP package
- JPL
  - LET/HET detector procurement; LET development/test
- GSFC
  - HET development/fabrication/detector test/system test
  - LET/HET on-board algorithm development
  - Overall SEP mechanical design and fabrication (e.g. detector, telescope, enclosure, and bracket design)
  - Overall SEP thermal design
  - SIT fabrication/assembly + SIT MISC

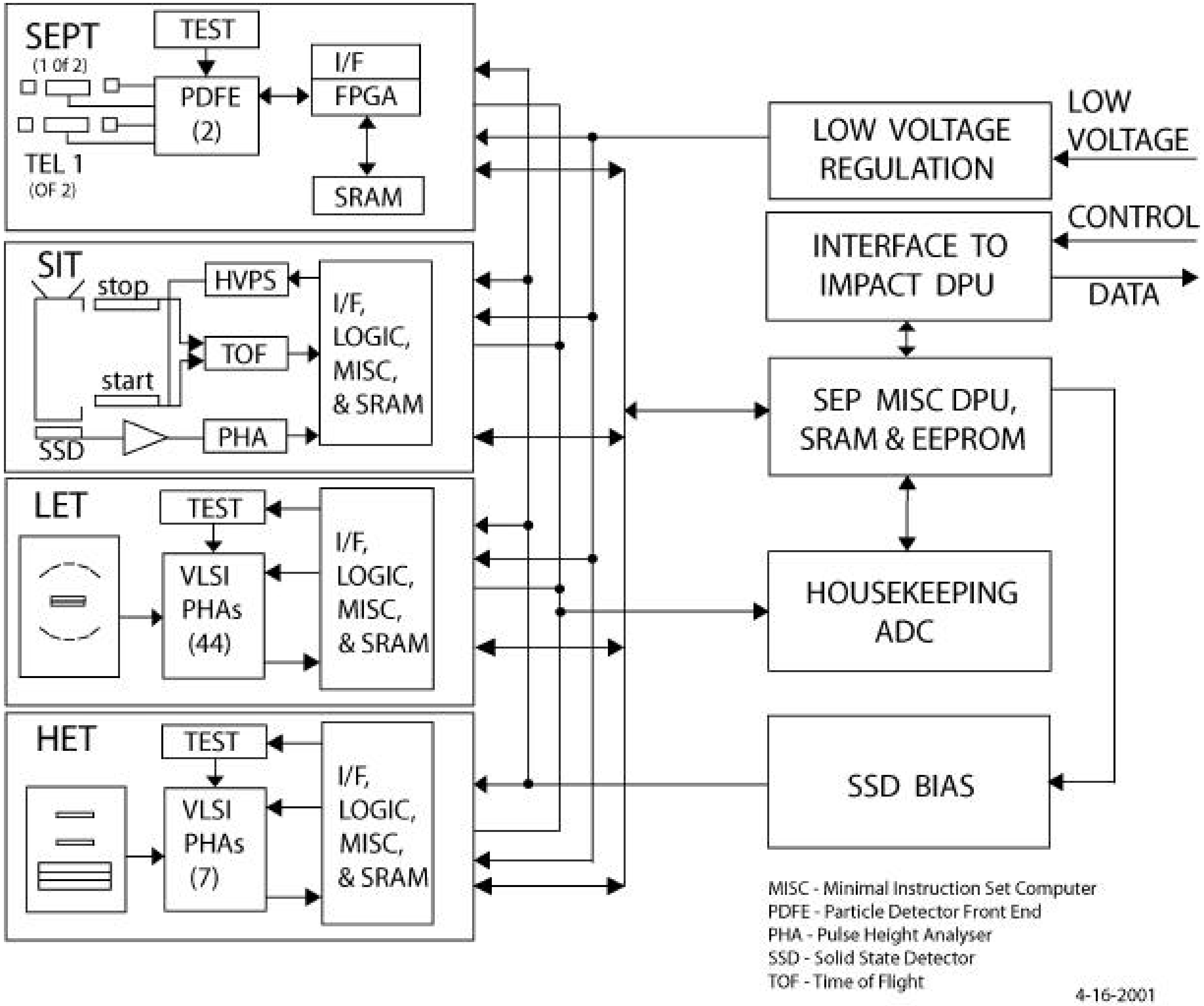
SEP Personnel

- Tycho von Rosenvinge, SEP Coordinator/HET Design/SEP Mechanical, GSFC, tycho@lheamail.gsfc.nasa.gov
- Bob Baker, Electronics Engineer, GSFC, baker@lheapop.gsfc.nasa.gov
- Mike Choi, Thermal Engineer, GSFC, mchoi@mscmail.gsfc.nasa.gov
- Rick Cook, SEP Lead Electronics Engineer, Caltech, wrc@srl.caltech.edu
- Alan Cummings, SEP Project Manager at Caltech, Caltech, ace@srl.caltech.edu
- Andrew Davis, On-board Software, Caltech, ad@srl.caltech.edu
- Peter Falkner, SEPT Electronics Engineer, ESTeC, Peter.Falkner@esa.int
- John Hawk, Thermal Engineer, GSFC, john.hawk@gsfc.nasa.gov
- Branislav Kecman, Electronics Engineer, Caltech, kecman@srl.caltech.edu
- Axel Korth, SIT TOF, MPI Lindau, korth@linmpi.mpg.de
- Horst Kunow, SEPT, UofKiel, kunow@kernphysik.uni-kiel.de
- Glenn Mason, SIT Design, UofMD, mason@sampex3.umd.edu
- Richard Mewaldt, LET Design, Caltech, rmewaldt@srl.caltech.edu
- Reinhold Mueller-Mellin, SEPT Design, UofKiel, mueller-mellin@kernphysik.uni-kiel.de
- Donald Reames, LET&HET On-board Algorithms, GSFC, reames@lheavx.gsfc.nasa.gov
- Sandy Shuman, SEP Mechanical Designer, GSFC, sandy@lheapop.gsfc.nasa.gov
- Trevor Sanderson, SEPT electronics, ESTeC, sanderson@estso3.estec.esa.ne
- Mark Wiedenbeck, LET & HET Detectors, JPL, Mark.E.Wiedenbeck@jpl.nasa.gov
- Peter Walpole, SIT Electronics Engineer, UofMD, walpole@sampex.umd.edu
- Kristin Wortman, On-board Software, GSFC, wortman@lheapop.gsfc.nasa.gov

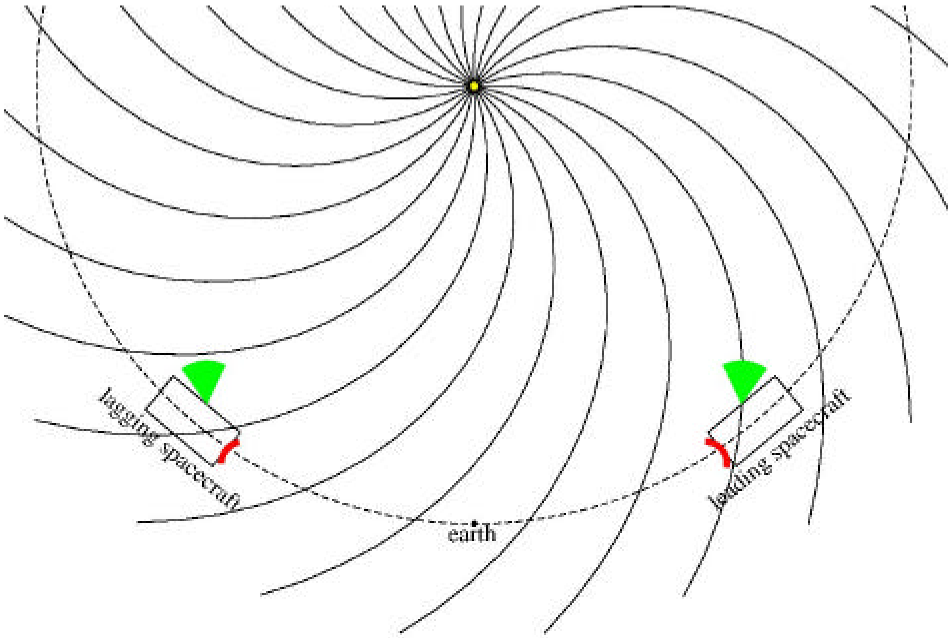
IMPACT Block Diagram



Overall SEP Block Diagram



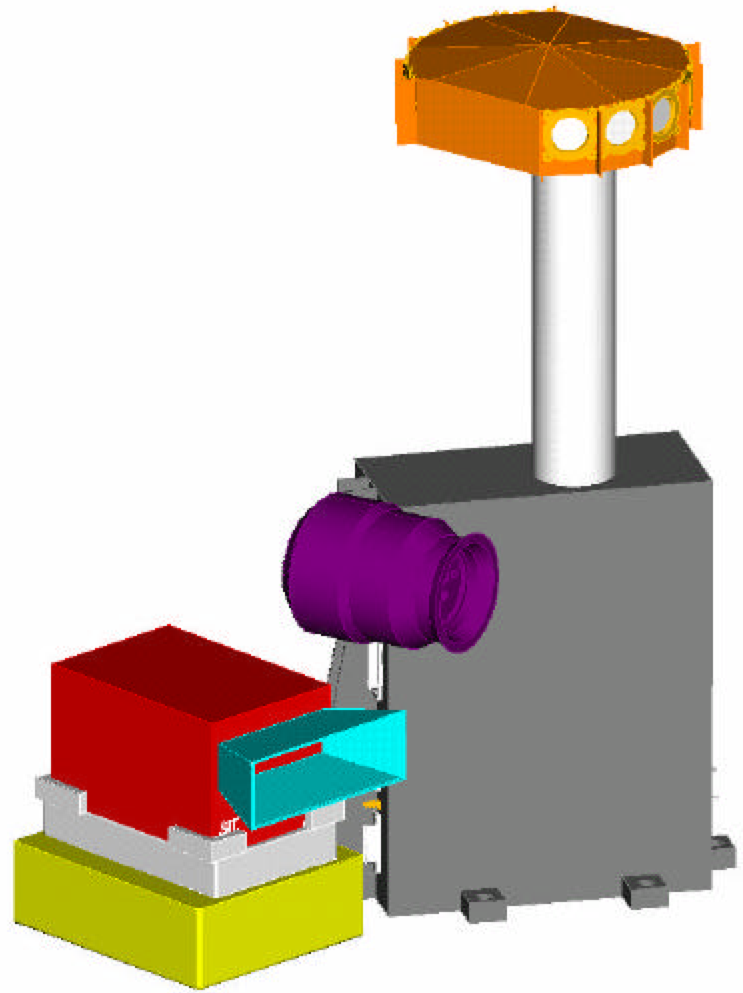
Parker Spiral Viewing



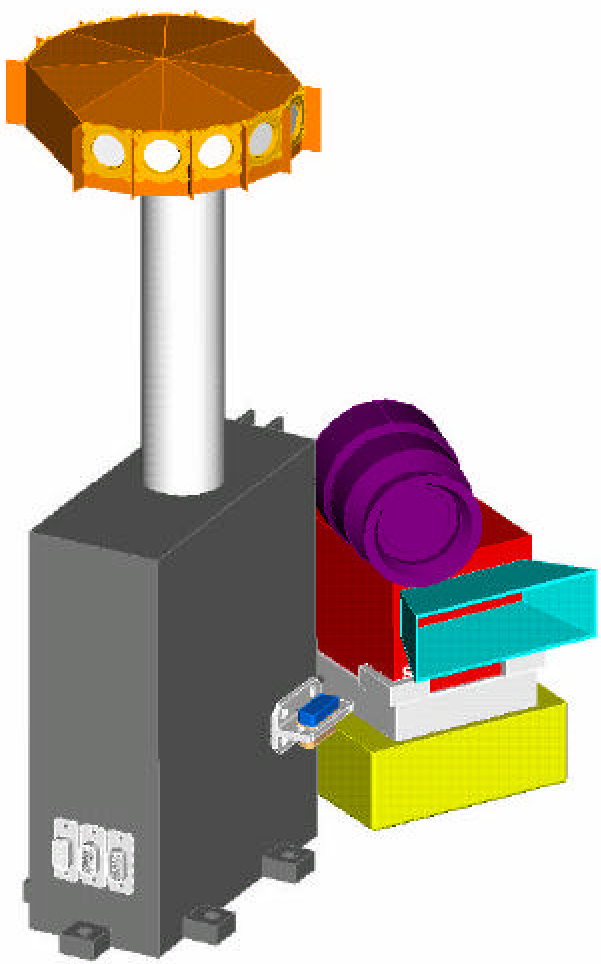
This figure shows magnetic field lines being carried radially out from the sun by the solar wind. These field lines are wrapped into a spiral (known as the Parker Spiral) due to the sun's rotation. Particles coming from the sun travel along the field lines, so the SEP Fields of View (FOVs, shown in green) need to be looking as depicted for the leading spacecraft.

The lagging spacecraft is predominantly a copy of the leading spacecraft rolled 180 degrees about the spacecraft-sun line. This points the dish antenna (shown in red) towards the earth and doesn't disturb the sun-pointing instruments. The figure shows that this 180 degree roll would cause the lagging SEP FOV to be pointing (incorrectly) perpendicular to the solar magnetic field lines. This means that the mounting of the SEP instruments cannot be the same on the leading and lagging spacecraft.

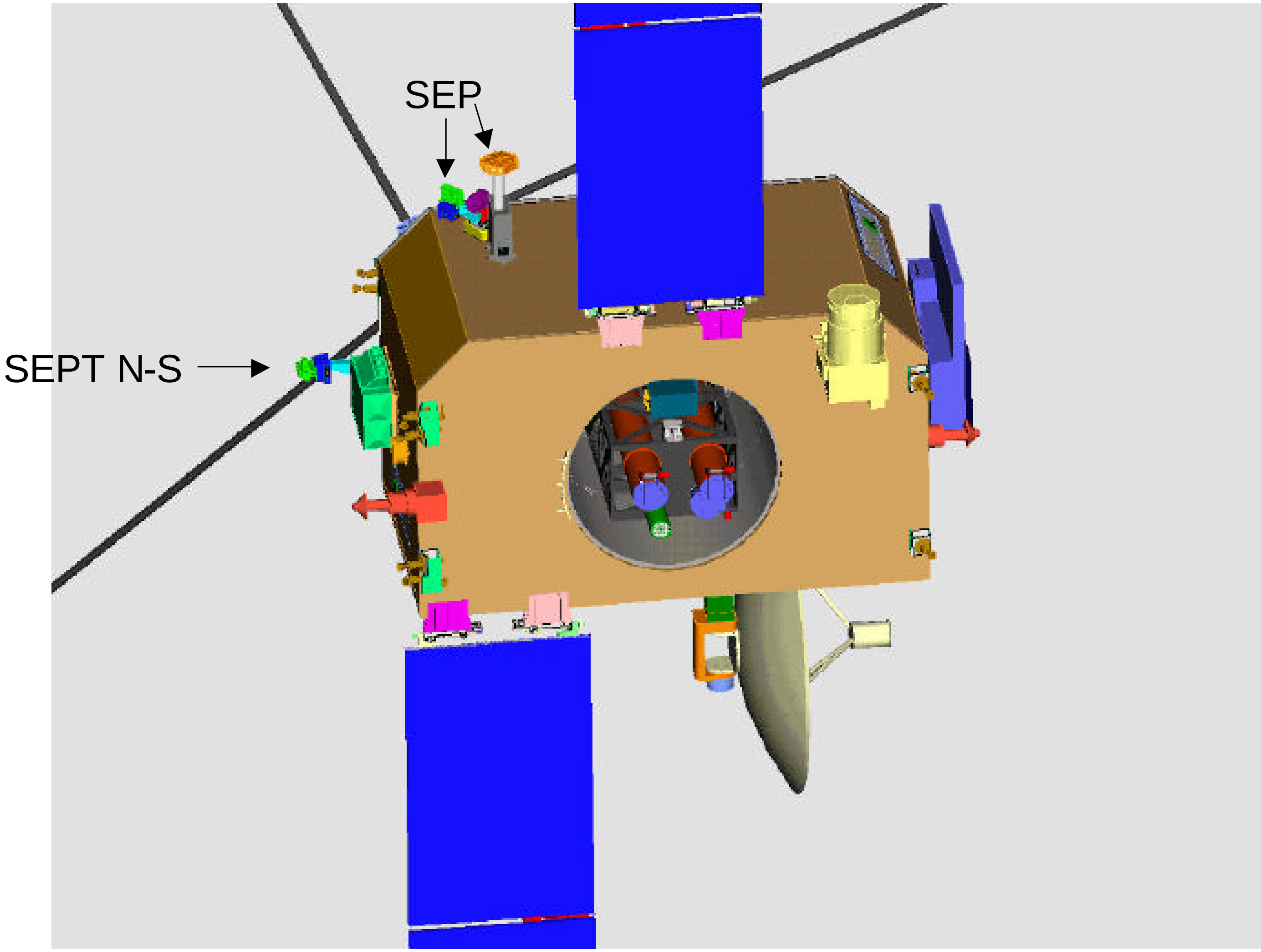
Ahead SEP Configuration



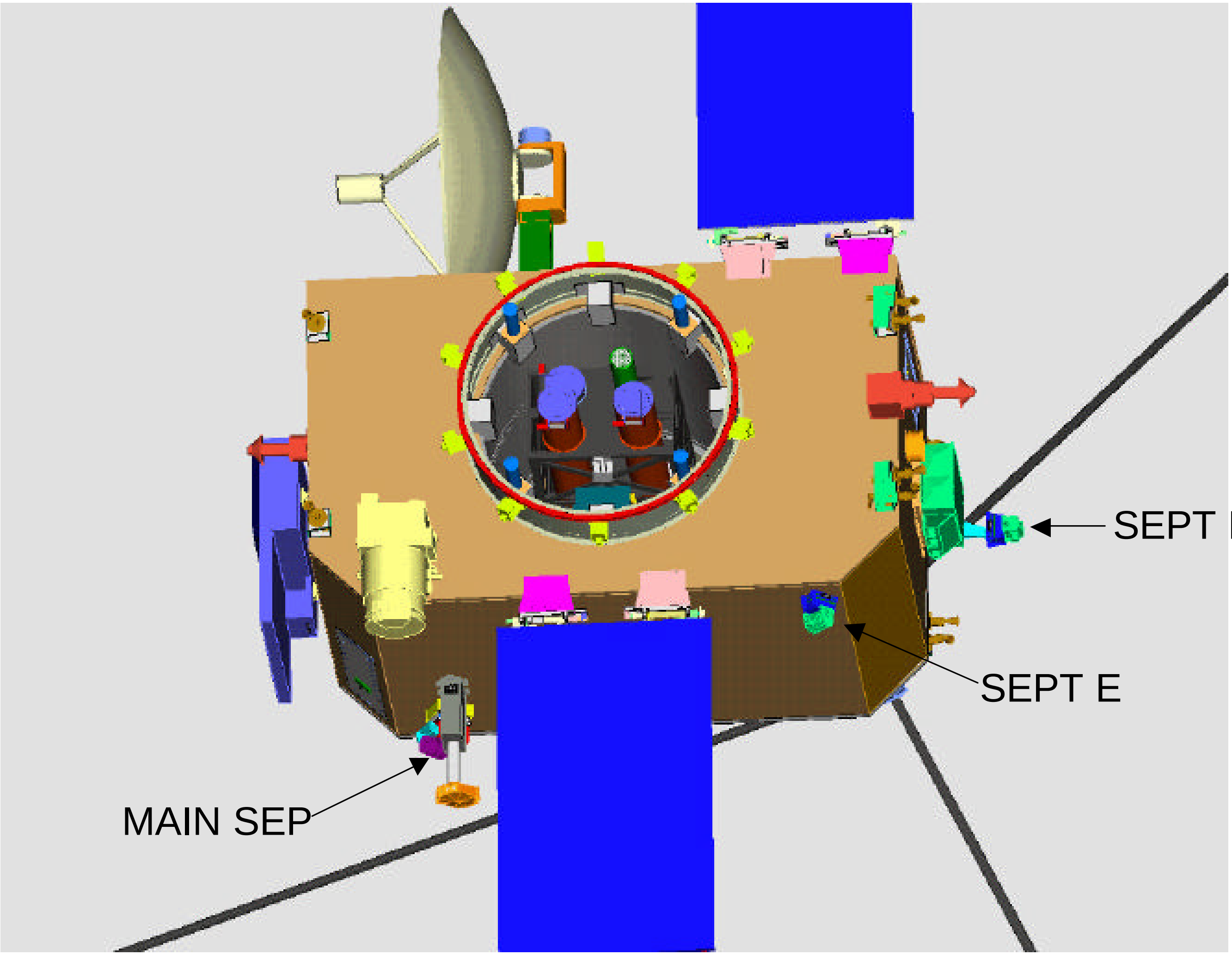
Behind SEP Configuration



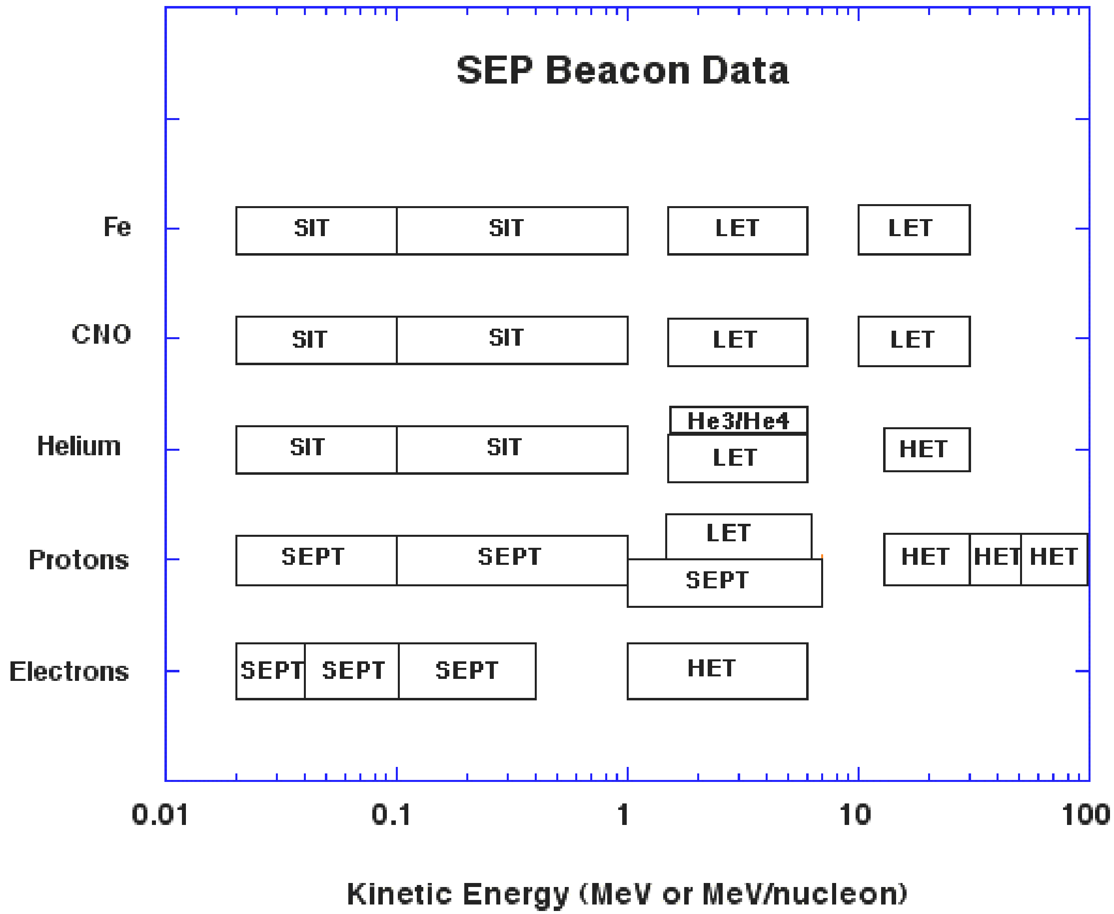
SEP Locations on the Ahead Spacecraft



SEP Locations on the Behind Spacecraft



SEP Beacon Data - I



SEP Beacon - II

SEP Beacon Data

SEP Sensor	Species	(MeV or MeV/nuc) E1	E2	Geometry Factor (cm2sr)	Number of Directions Summed Over	Time Resolution (sec)	Min. Observable 1-minute Flux (/cm2sr.sec.MeV)	bps
SIT	He	0.02	0.1	0.3	1	60	6.9E-01	0.27
		0.1	1	0.3	1	60	6.2E-02	0.27
	CNO	0.02	0.1	0.3	1	60	6.9E-01	0.27
		0.1	1	0.3	1	60	6.2E-02	0.27
	Fe	0.02	0.1	0.3	1	60	6.9E-01	0.27
		0.1	1	0.3	1	60	6.2E-02	0.27
								0.27
SEPT	Electrons	0.02	0.04	0.8	4	60	1.0E+00	0.27
		0.04	0.1	0.8	4	60	3.5E-01	0.27
		0.1	0.4	0.8	4	60	6.9E-02	0.27
	Ions	0.02	0.12	0.96	4	60	1.7E-01	0.27
	(mostly	0.12	1	0.96	4	60	2.0E-02	0.27
	protons)	1	7	0.96	4	60	2.9E-03	0.27
LET	Protons	1.5	6	0.9	10	60	4.1E-03	0.27
	Helium	1.5	6	4.5	10	60	8.2E-04	0.27
	3He/4He	2	6	2	10	60	2.1E-03	0.27
	CNO	2	6	4.5	10	60	9.3E-04	0.27
	CNO	10	30	4.5	10	60	1.9E-04	0.27
	Fe	2	6	4.5	10	60	9.3E-04	0.27
	Fe	10	30	4.5	10	60	1.9E-04	0.27
HET	Electrons	1	4	0.5	1	60	1.1E-02	0.27
	Protons	13	30	0.7	1	60	1.4E-03	0.27
		30	50	0.7	1	60	1.2E-03	0.27
		50	100	0.7	1	60	4.8E-04	0.27
	He	13	30	0.7	1	60	1.4E-03	0.27
								6.67

SEP Milestone Schedule

Peer Review, SEP	4/19/01
Phase B start	6/1/01
Peer Review, IDPU	6/13/01
VLSI chip definition to SIT & HET	6/27/01
Peer Review, Wrapup	8/2/01
PDR	9/11/01
Confirmation Review	3/4/02
Phase CD start	3/4/02
Flight VLSI chips delivery to SIT & HET	4/17/02
All flight detectors ordered	4/29/02
LVPS EM available from UCB	6/17/02
Prelim. I/F test with IDPU	10/4/02
CDR	11/4/02
Detector testing complete	2/3/03
GSE ready	4/28/03
HET delivery to Caltech	6/11/03
Boards fabricated and tested	7/4/03
Integration of LET complete	7/23/03
SIT delivery to Caltech	7/30/03
Integration of HET complete	9/3/03
SEPT delivery to Caltech	9/10/03
Integration of SIT complete	10/22/03
Final flight firmware complete	10/22/03
Integration of SEPT complete	12/10/03
Integration of LET/HET/SIT/SEPT complete	2/4/04
Ready to integrate SEP with IDPU	2/23/04
End-to-end test at accelerator	5/10/04
SEP Env Test Starts	5/31/04
IMPACT EMC Test Starts	6/25/04
Functional/env. testing complete	9/10/04
SEP Delivery to UCB	9/10/04
Pre-ship review	9/27/04
Launch	12/8/05

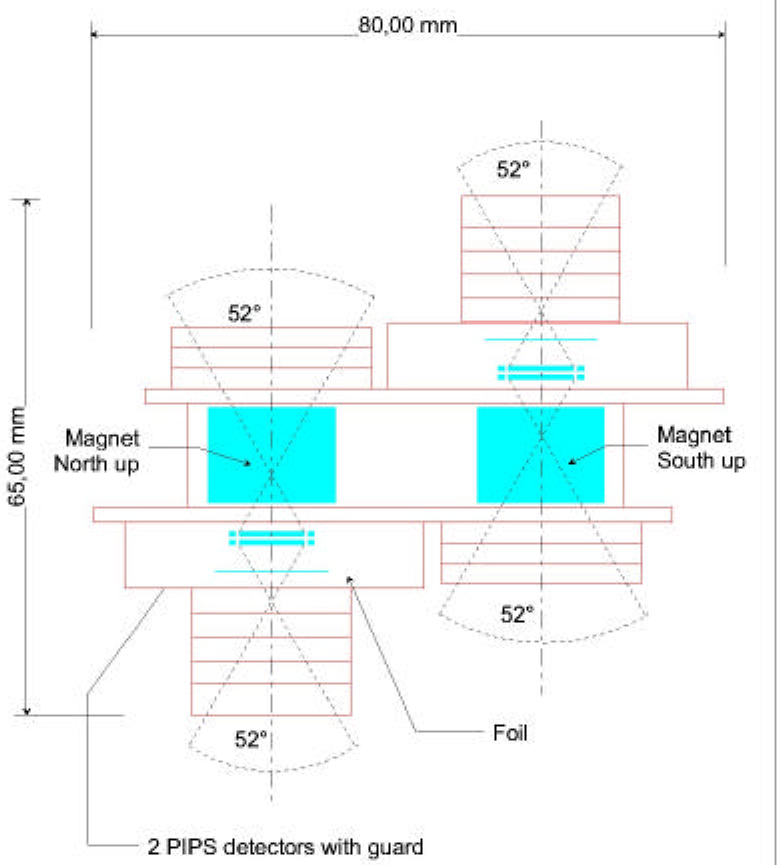
Controlling Documents

- **IMPACT Phase A Report covers the top level instrument performance requirements**
- **IMPACT/Spacecraft ICD covers the spacecraft interface**
- **IMPACT Serial Interface document covers the data interface between SEP and the IDPU**
- **IMPACT PAIP covers the performance assurance requirements**
- **STEREO EMC and Contamination Control plans**

Solar Electron Proton Telescopes (SEPT)

University of Kiel
ESTeC

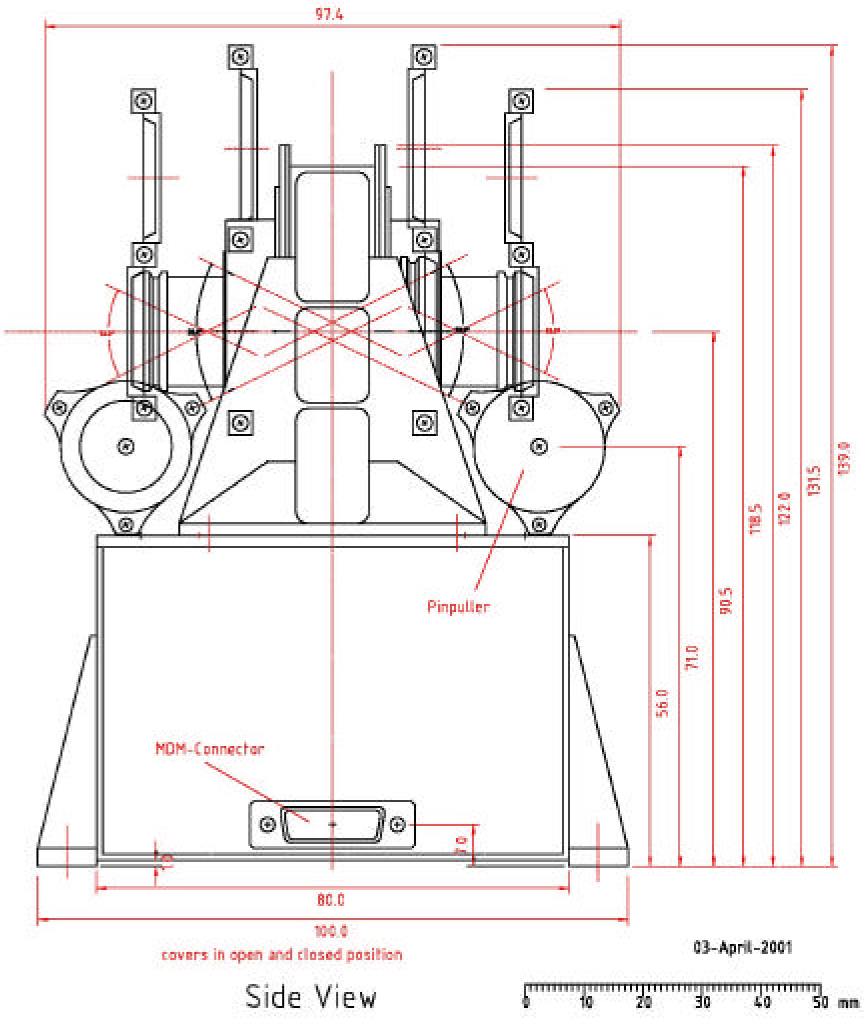
SEPT Telescope Schematic



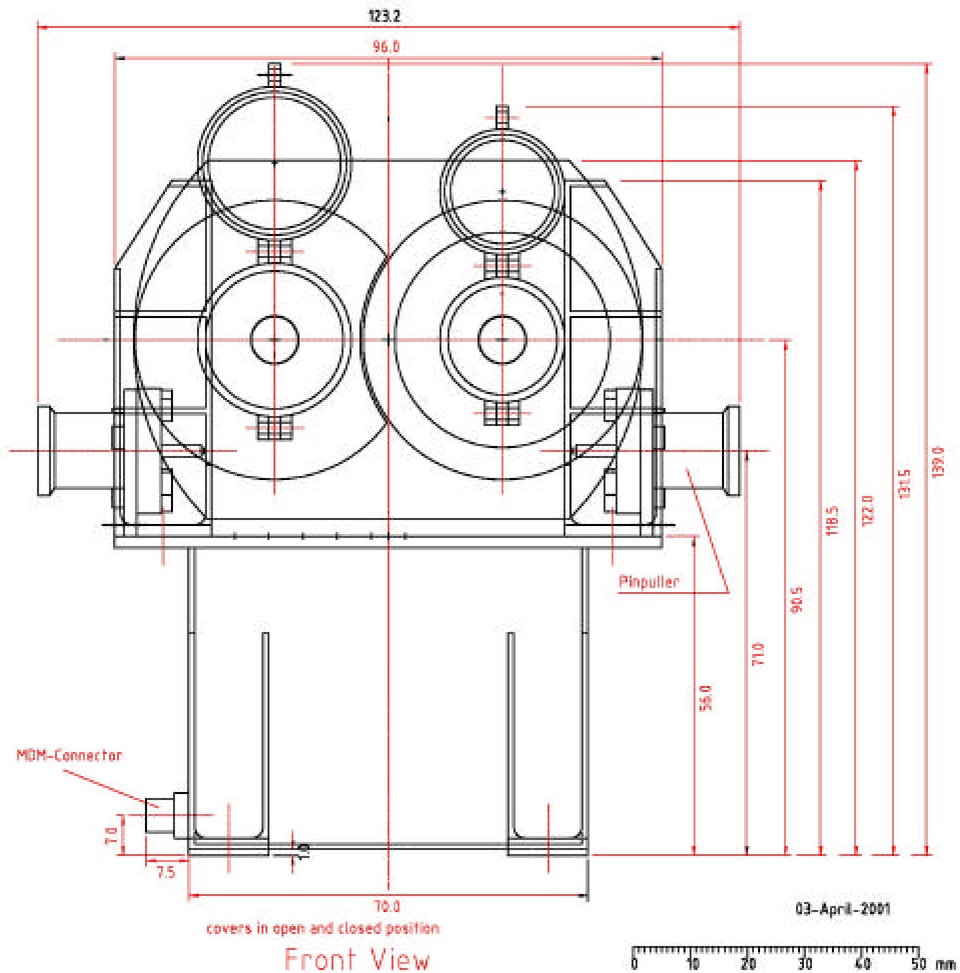
SEPT Performance Requirements

Description	Goal	Requirement
FOV	2 sets of oppositely directed 52 degree cones each for electrons and protons	2 sets for electrons and protons, each with: 2 oppositely directed view cones in-ecliptic, 2 oppositely directed view cones off-ecliptic, 45 degree full opening angle
Energy	20-400 keV electrons, 20-7000 keV protons	30-400 keV, electrons 30-2000 keV, protons
Energy Resolution (Telemetry)	20% electrons, 20% protons	30%, electrons 30%, protons
Geometric Factor	0.52 cm^2 ster, electrons, 0.68 cm^2 ster, protons	0.4 cm^2 ster, electrons, 0.4 cm^2 ster, protons
Background	< 0.2 counts/s on ground, 20°C	< 2 counts/s on ground, 20°C
Max Event Rate	25,000 counts/s at 2.2 MeV 250,000 counts/s at 55 keV	25,000 counts/s at 2.2 MeV 250,000 counts/s at 55 keV
Time Resolution	60 sec	60 sec

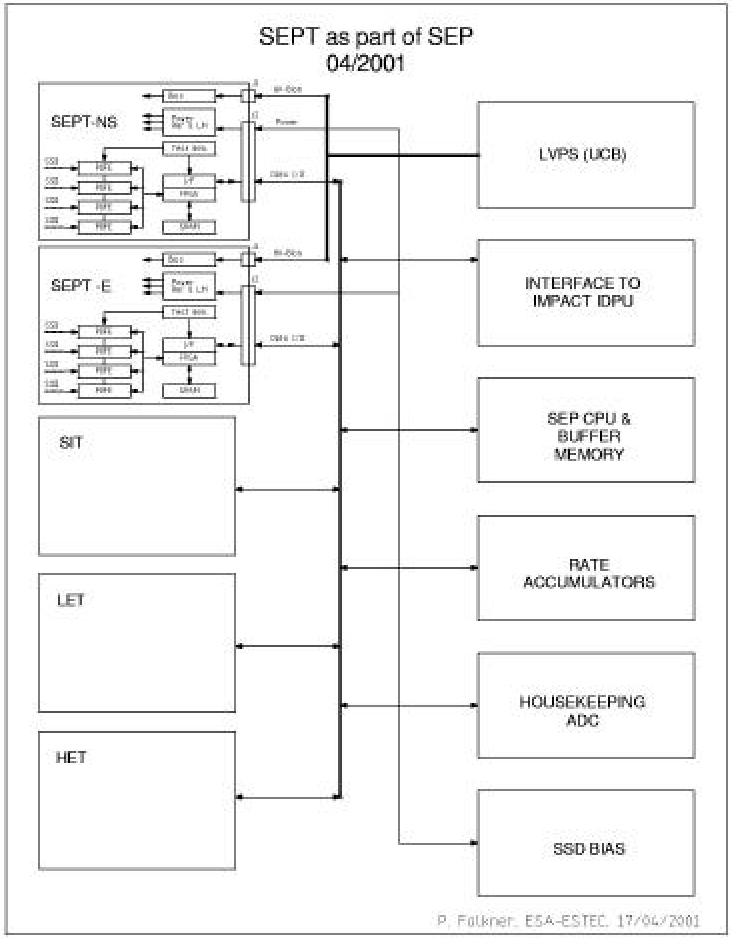
SEPT Side View



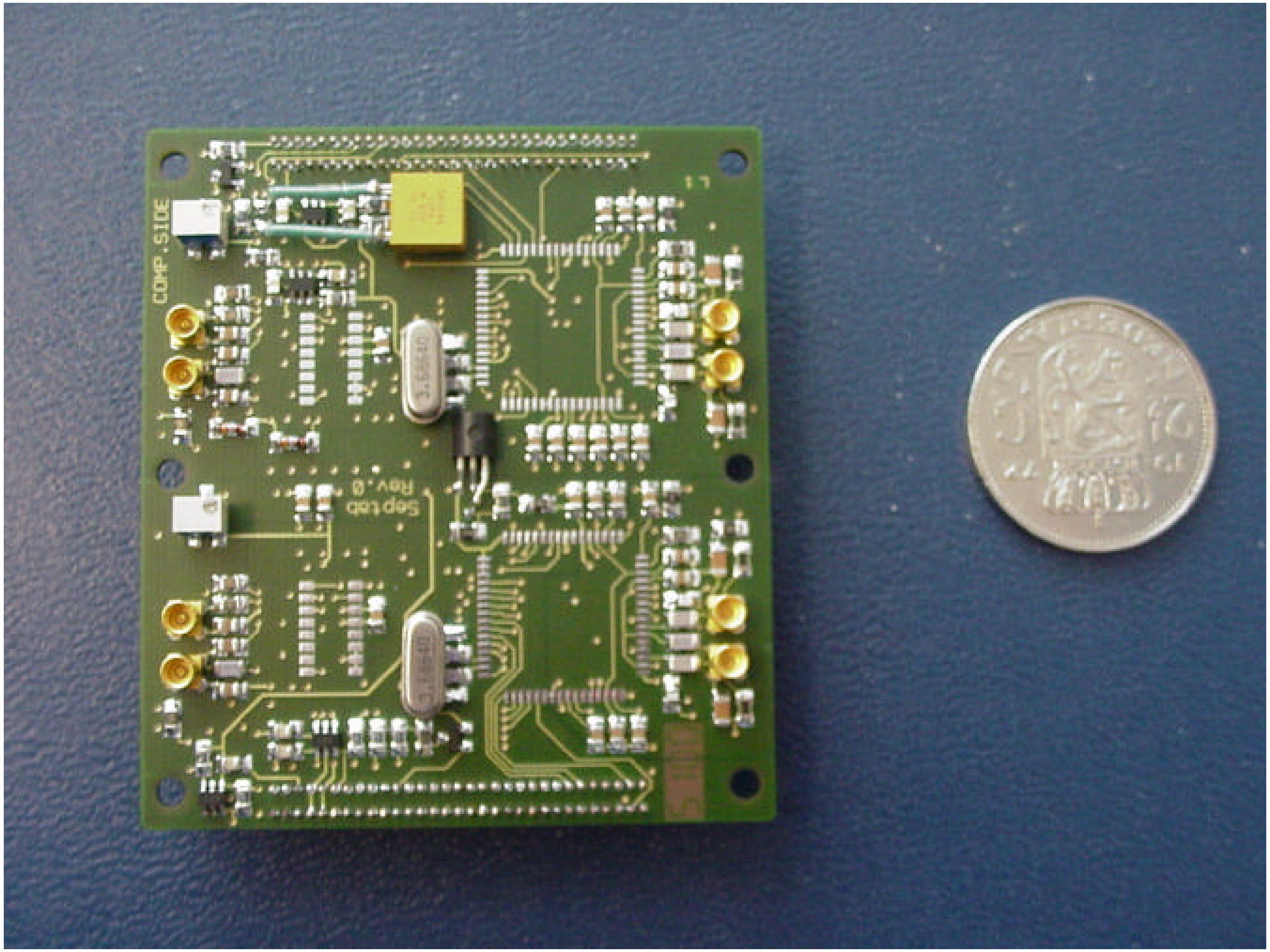
SEPT Front View



SEPT Block Diagram



SEPT Prototype Analog Electronics Board



SEPT System

SEPT consists of *(numbers given per S/C)* :

–SEPT-E:	2 double-ended telescopes	UoK
–SEPT-NS:	2 double-ended telescopes	UoK
–2 sets of pigtails to SEPT Electronics		UoK
–2 housing boxes for SEPT Electronics		UoK
–1 bracket for SEPT-NS		GSFC
–2 sets of analog and digital electronics		ESTEC
–2 sets of interconnecting harness to SEP-DPU		GSFC

Preliminary SEPT Hazardous Materials List

Instrument/Equipment : IMPACT/SEPT-E or -NS (GSE)				Prepared by: R. Mueller-Mellin		Doc-Number: Issue/Rev.: 1; Date: 28-Aug-01		
item #	name & type of product	manufacturer, specification	processing parameters	hazardous radiation	application & where used	environment	activity	remarks, approval-reference
1	^{207}Bi (Bismuth)	Amersham Buchler, Braunschweig, Germany	sealed	electron 480, 967, 1047 keV	aperture cover (red tag item)	ambient	1 µCi	non-flight item, used during ground testing, detector calibration, detector aliveness
2	^{60}Co (Cobalt)	Amersham Buchler, Braunschweig, Germany	sealed	gamma 1173, 1332 keV	aperture cover (red tag item)	ambient	10 µCi	non-flight item, used during ground testing, detector calibration, detector aliveness

Preliminary SEPT Materials and Processes List (1 of 3)

Instrument/Equipment : **IMPACT/SEPT Electronics-Box** (E or NS)				Prepared by: J. Falenski, E. Rode, R. Mueller-Mellin		Doc-Number: Issue/Rev.: 1; 28-Aug-01; page 1 of 2		
item #	name & type of product, form & condition	manufacturer, specification	processing parameters	outgassing or SCC-res., data & refer.	application & where used	envi-ronm ent	size cod e	remarks, approval-reference
1	Al-alloy 3.3214	air tec, Mülheim/ Ruhr	metal sheet, block material (Alodine)	PSS-01-736	structure			high corrosion-resistant
2	V4A 1.4401 Screws, nuts, washers	Hummer + Rieß DIN X5CrNiMo 1810	produced by machinin g		structure, PC-boards			non-magnetic non corroding
3	Polyimide	PRINTCA Denmark			PC-boards			
4	Epoxy-Glue 3M2216				supports and inter-board connectors			

Preliminary SEPT Materials and Processes List (2 of 3)

Instrument/Equipment : **IMPACT/SEPT Electronics-Box** (E or NS)				Prepared by: J. Falenski, E. Rode, R. Mueller-Mellin		Doc-Number: Issue/Rev.: 1; 28-Aug-01; page 1 of 2		
item-#	name & type of product, form & condition	manufacturer, specification	processing parameters	outgassing or SCC-res., data & refer.	application & where used	envi-ronment	size code	remarks, approval-reference
5	Parylene C				Coating of PCBs		W3	Conformal coating
6	Solder Sn 63				electronics			
7	Electrodag 501	Acheson			box walls			thermal paint
8	Diallyl-Phthalate				Encapsulation of connectors		W2	
9	TFE Fluorcarbon				Encapsulation of connectors		W2	
10	PTFE				Coaxial cables		W2	
11	FEP				Coaxial cables		W2	

Preliminary SEPT Materials and Processes List (3 of 3)

Instrument/Equipment : **IMPACT/SEPT Electronics-Box** (E or NS)				Prepared by: J. Falenski E. Rode		Doc-Number: Issue/Rev.: 1; 28-Aug-01; page 2 of 2		
item #	name & type of product, form & condition	manufacturer, specification	processing parameters	outgassing or SCC-res., data & refer.	application & where used	environment	size code	remarks, approval-reference
12	Vespel, Polyimide	Du Pont (USA)			underneath mounting lugs			thermal insulator
13	Process ESA/PSS-01 738							soldering of surface mounted components

The size code is denoted by:	
V0	0……….1 [cm^3]
A1	1……....10 [cm^2]
A2	10........100 [cm^2]
A3	100…1000 [cm^2]
W1	1……....10 [g]
W2	10……100 [g]
W3	100…1000 [g]

Preliminary SEPT Sensor Materials and Processes List (1 of 3)

Instrument/Equipment : **IMPACT/SEPT Sensor** (E or NS)				Prepared by: J. Falenski, E. Rode, R. Mueller-Mellin		Doc-Number: Issue/Rev.: 1; 28-Aug-01		
item #	name & type of product, form & condition	manufacturer, specification	processing parameters	outgassing or SCC-res., data & refer.	application & where used	envi-ronment	size code	remarks, approval-reference
1	Al-alloy 3.3214 AA 6061	air tec, Mülheim/Ruhr	round mat., plate mat.	PSS-01-736	sensor housing			high corrosion-resistant
2	V4A 1.4401 Screws, nuts, washers	Hummer + Rieß DIN X5CrNiMo 1810	produced by machining		sensor housing			non-magnetic non corroding
3	Delrin 500, Polyacetal Thermoplast	Du Pont (USA)		TML=0.24% VMC=0%	sensor housing			insulation
4	Viton Elastomer Rubber	Du Pont (USA)		TML=0.5% RML=0.2% CVCM=0.02% PSS-01-702	O-rings in flanges			
5	Parylene Foil (aluminized)				sensor aperture			

Preliminary SEPT Sensor Materials and Processes List (2 of 3)

Instrument/Equipment : **IMPACT/SEPT Sensor** (E or NS)				Prepared by: J. Falenski, E. Rode, R. Mueller-Mellin		Doc-Number: Issue/Rev.: 1; 28-Aug-01		
item #	name & type of product, form & condition	manufacturer, specification	processing parameters	outgassing or SCC-res., data & refer.	application & where used	environment	size code	remarks, approval-reference
6	Permanent magnet NdFeB	Vakuum-schmelze Hanau			sensor			Vacodym VD745HR
7	Soft iron yoke	Vakuum-schmelze Hanau			sensor			Vacoflux 50
8	Epoxy-Glue Eccobond 55	Emerson u. Cuming (B)		TML=0.7% RML=0.5% CVCM=0.02%	magnet system			high corrosion-resistant
9	Shrinking Tube Thermofit Kynar RT-76	Raychem, Pennwalt MIL-I-23053 C/8			mounting of harness		W1	
10	Diallyl-Phthalate				Encapsulation of connectors		W2	
11	TFE Fluorcarbon				Encapsulation of connectors		W2	

Preliminary SEPT Sensor Materials and Processes List (3 of 3)

Instrument/Equipment : **IMPACT SEPT Sensor** (E or NS)				Prepared by: J. Falenski, E. Rode, R. Mueller-Mellin		Doc-Number: Issue/Rev.: 1; 28-Aug-01		
item #	name & type of product, form & condition	manufacturer, specification	processing parameters	outgassing or SCC-res., data & refer.	application & where used	Environment	size code	remarks, approval-reference
12	PTFE				Triaxial cables		W2	
13	FEP				Triaxial cables		W2	
14	Silicon	Canberra Belgium			detectors			
15	Epoxy, reinforced by glass fiber	Canberra Belgium			detector mount			PC board
16	DURAL	Canberra Belgium			detector inner housing			aluminium alloy

The size code is denoted by:	
V0	0………..1 [cm^3]
A1	1……....10 [cm^2]
A2	10........100 [cm^2]
A3	100…1000 [cm^2]
W1	1……....10 [g]
W2	10……100 [g]
W3	100…1000 [g]

SEPT Concerns

- Concern about solar heat input solved: covers for all apertures baselined (TiNi actuators)
- Concern about scattered light in apertures solved: ohmic side of detectors face open space, can be made light-tight, penalty: increase of lower energy threshold
- Concern about viewing cone obstructions continue for SEPT-NS, mitigated by reduction of cone angle from 60° to 52°
- Cross talk between inner segment (D1) and outer ring (G1)
  - Solution: insert narrow guard ring (C1)
  - Penalty: 3 coax cables per detector instead of 2
- Cross talk between D1 and D2, no solution yet, calculate capacitive coupling using known area (52 mm^2) and distance (600 μm)
- Purging required

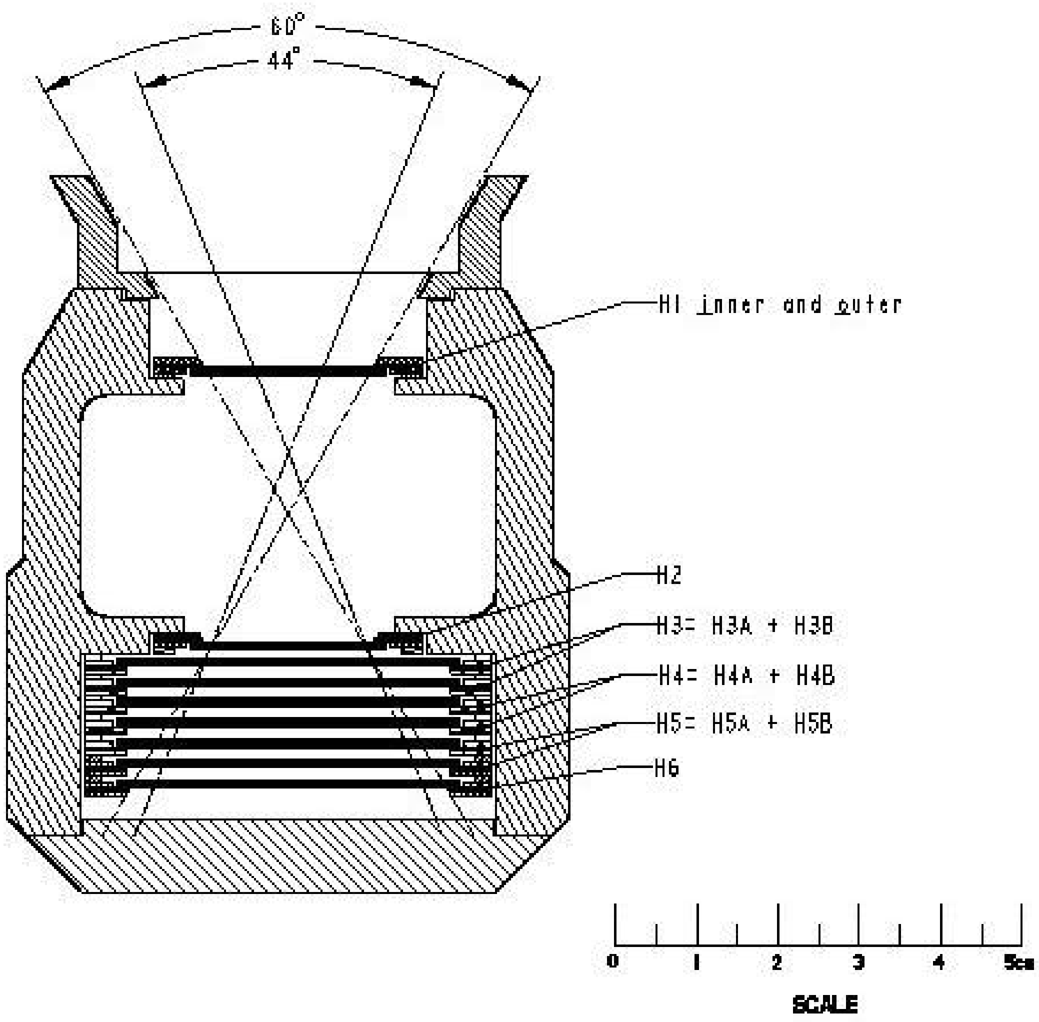
High Energy Telescope (HET)

GSFC
Caltech
JPL

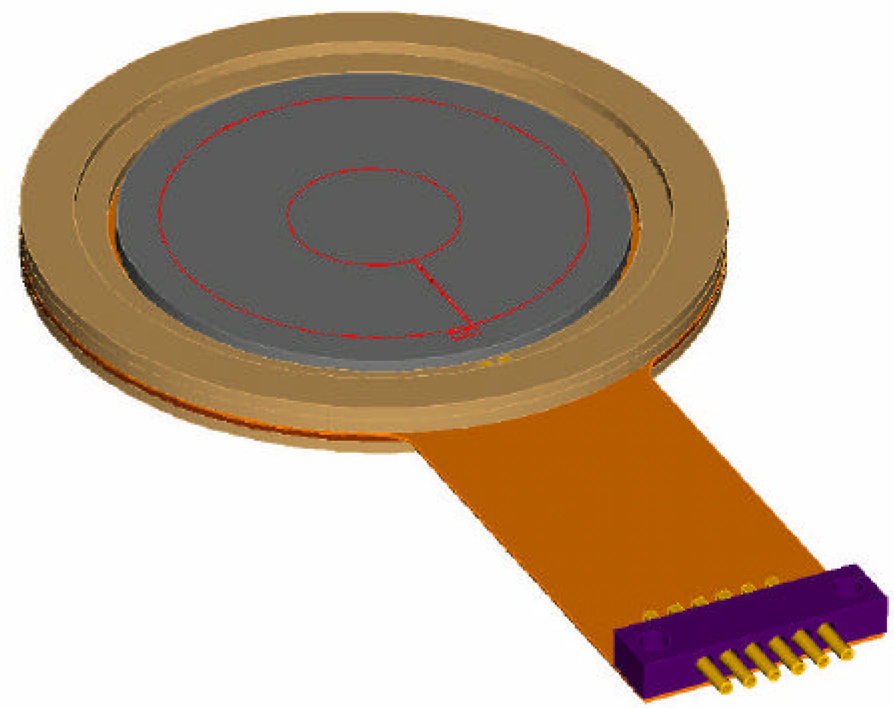
HET Performance Requirements

Description	Goal	Requirement
FOV (full angle)	58 degree cone	50 degree cone
Energy Range (MeV/nucleon)	e: 1 - 6 H, He: 13 - 100 ^{3}He: 16 – 50 ~30 to 80 for 5 < Z < 27	1 – 8 13 – 40 16 – 40 ~30 to 80 for 5 < Z < 15
Geometric Factor, cm^2 ster	0.7	0.5
Element Resolution, dZ (rms), for stopping particles	< 0.3 for 16 < Z < 26	< 0.2 for 1 < Z < 15
^{4}He Mass Resolution	<0.20 amu	<0.25 amu
Max Event Rate	5000 events/sec	1000 events/sec
Energy Binning	Eight intervals per species	Six intervals per species
Species Binning	Add 15 < Z < 27	H, ^{3}He, ^{4}He, 5<Z<15, Electrons
Time Resolution	15 minutes 1 prioritized events/sec	15 minutes 0.3 prioritized event/sec
Beacon Telemetry:	1 minute H, He, e	1 minute H, He, e

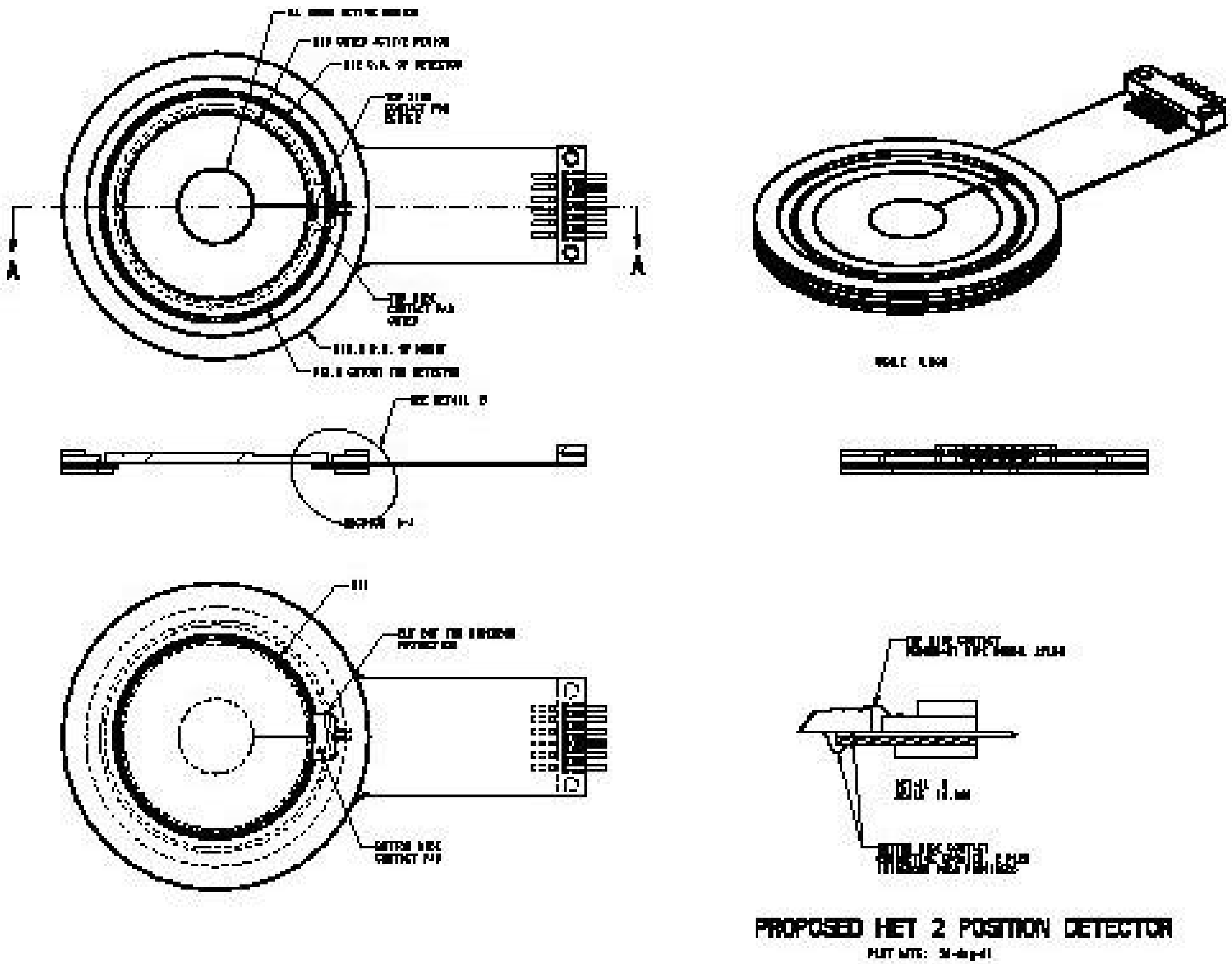
HET Telescope Schematic



HET H1 Detector



HET H1 Detector Schematic



HET Thresholds and Gains

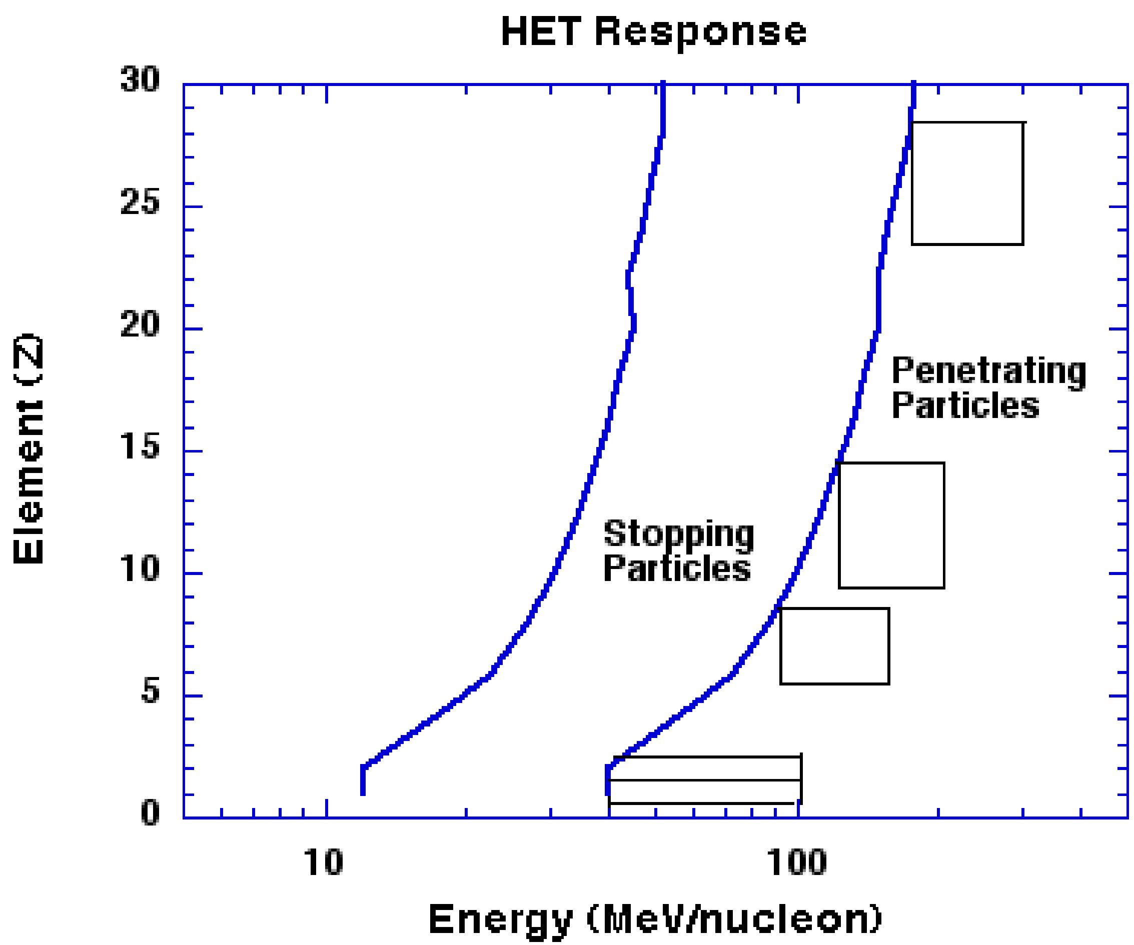
																	8.30.01
							HET Thresholds and Gains										
					Minimum	Nominal	Min.	Hi-gain	Hi-gain	Delta (2)	Max.	Min.		Nom (3)	Lo-gain	Lo-gain	
			Detect.	Est. (1)	Thresh	Hi-gain	Hi-gain	Full	channel	Threshold	Hi-gain	Lo-gain	Delta (2)	Hi-Rate	Full	channel	Total
	Area	Thick	Cap.	Noise	(MeV)	Thresh	Setting	Scale	width	Adjust.	Thresh	Thresh	Adjust.	Thresh	Scale (4)	width	Dynamic
Detector	cm2	(micron)	(pf)	(MeV)	(=5 x n)	(MeV)	(MeV)	(MeV)	(MeV)	(MeV)	(MeV)	(MeV)	(MeV)	(MeV)	(MeV)	(MeV)	Range (5)
H1i	0.5	1000	6	0.037	0.185	0.20	0.1841	92	0.045	0.006	5.84	3.68	0.09	0.20	1841	0.899	9951
H1o	2.64	1000	30	0.037	0.185	0.20	0.1841	92	0.045	0.006	5.84	3.68	0.09	16	1841	0.899	9951
H2	3.14	1000	36	0.037	0.185	0.20	0.1841	92	0.045	0.006	5.84	3.68	0.09	0.20	1841	0.899	9951
H3,H4,H5	12	2000	273	0.080	0.400	0.45	0.3989	199	0.097	0.012	12.65	7.98	0.19	0.45	3989	1.948	9973
H6	12	1000	137	0.037	0.185	0.20	0.1841	92	0.045	0.006	5.84	3.68	0.09	0.20	1841	0.899	9951

The maximum H1, H2 energy-loss to meet the science requirements is ~75 MeV; the maximum of interest is ~3000 MeV

The maximum H3, H4, H5 energy-loss to meet the science requirements is ~100 MeV; the maximum of interest is ~4000 MeV

Notes:
(1) Noise estimated by W. R. Cook, taking into account all known contributions
(2) Nominal thresholds can be adjusted (by command) to accommodate range of thicknesses and noise
(3) For some L1i and L2, and for L1o, L3o, and H1o the low-gain thresholds will be raised during very high-rate periods
(4) Dynamic range = 500 for both low and high gain; nominal high/low gain factor = 20
(5) Ratio of Lo-gain full scale to minimum hi-gain threshold (5 times noise)

HET Energy/Particle Response



HET Counting Rates

Proton Counting Rates Based Upon the 14 July 2000 Event Peak Intensity	
H1i Singles Rate	17,000/sec
H1i + H1o Singles Rate	100,000/sec
H1i.H2 Coincidence Rate	1400/sec
(H1i + H1o).H2 Coincidence Rate	8000/sec

HET Operation During High-Rate Periods

Requirement: Provide composition and energy spectra measurements over conditions ranging from quiet-time to the largest solar events

Issue: During very high-rate periods (e.g., peak of Bastille Day 2000 event) the single-detector count rates, especially on the front detector, will exceed 100,000/sec

Approach (Similar to LET):

- **H1 detector has bull's-eye design with smaller central area**
- **Collimation of H1 detector to shield against wide-angle protons**
- **Sides of telescope shielded to reduce H2 to H6 count rates**
- **Adjust threshold on H1o to reduce overall count rate while maintaining energy and species coverage**

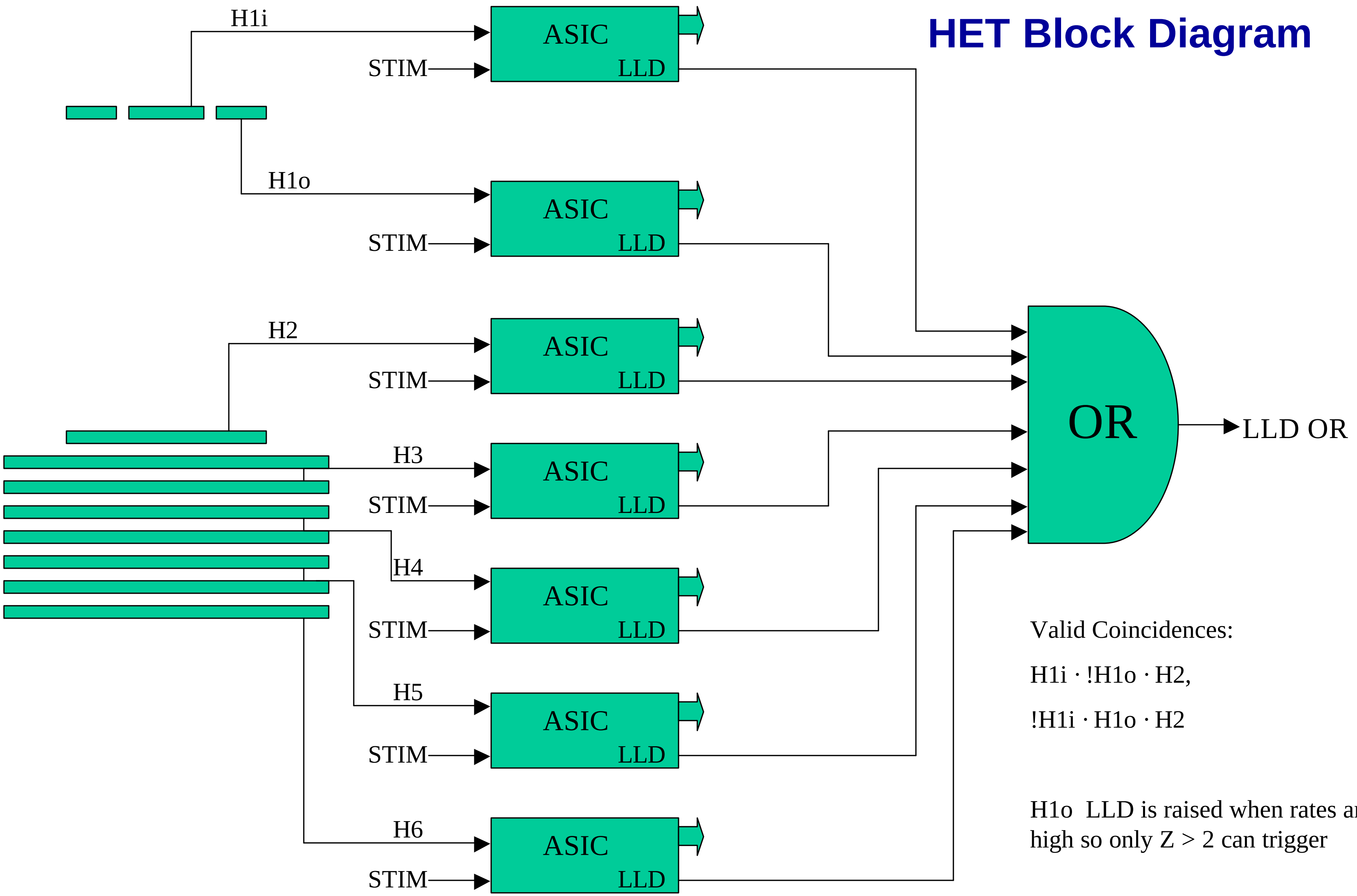
HET Operation During High-Rate Periods … Cont

- **Threshold adjusted by ignoring high-gain response on selected detectors**
- **Adjustments controlled on-board by "OR" of count-rates from detectors that are not adjusted (H1i, H2 - H6).**

Implementation:

- **H1o threshold raised from 0.2 to ~16 MeV when singles rates reach TBD value.**

HET Block Diagram



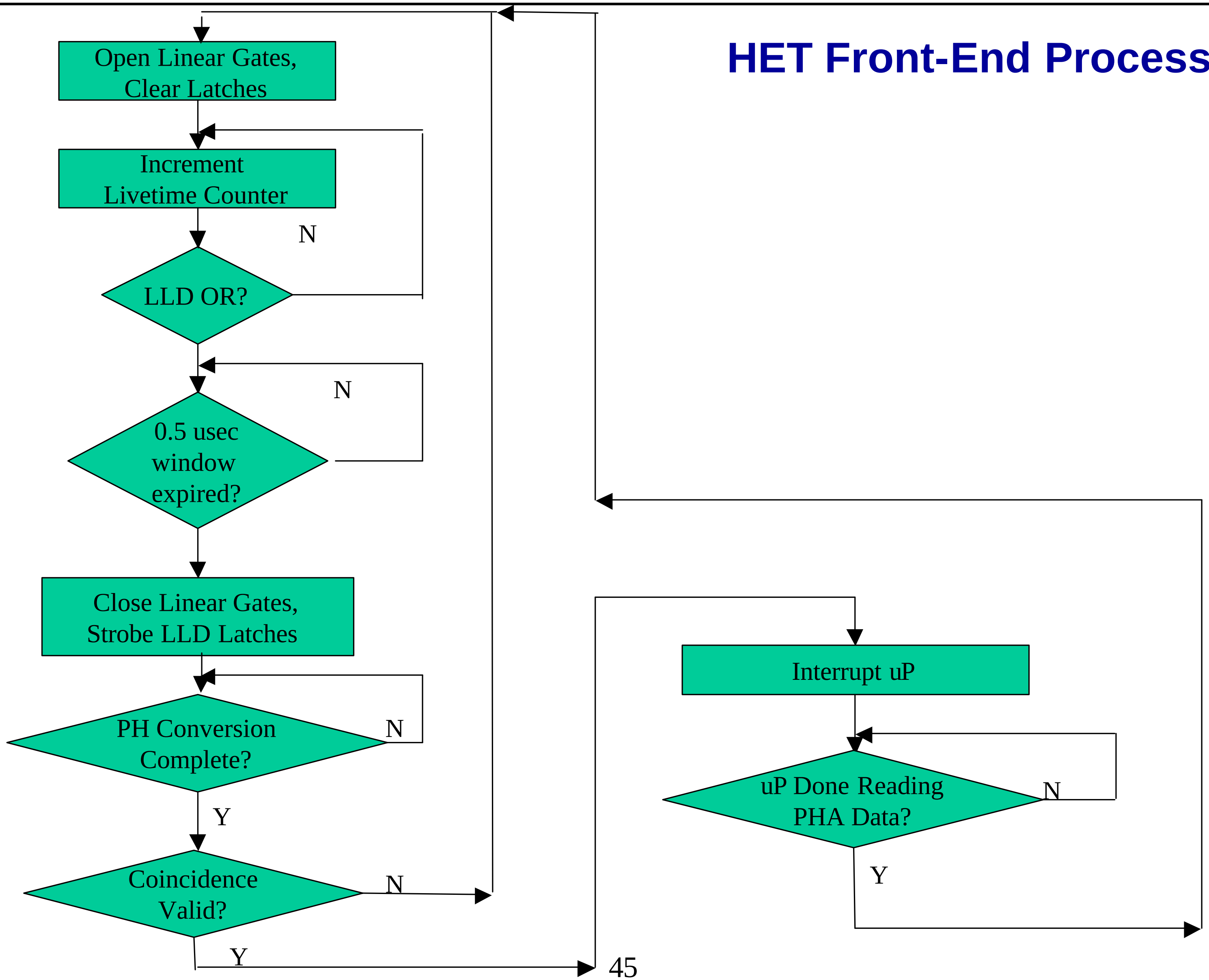
Valid Coincidences:

H1i · !H1o · H2,

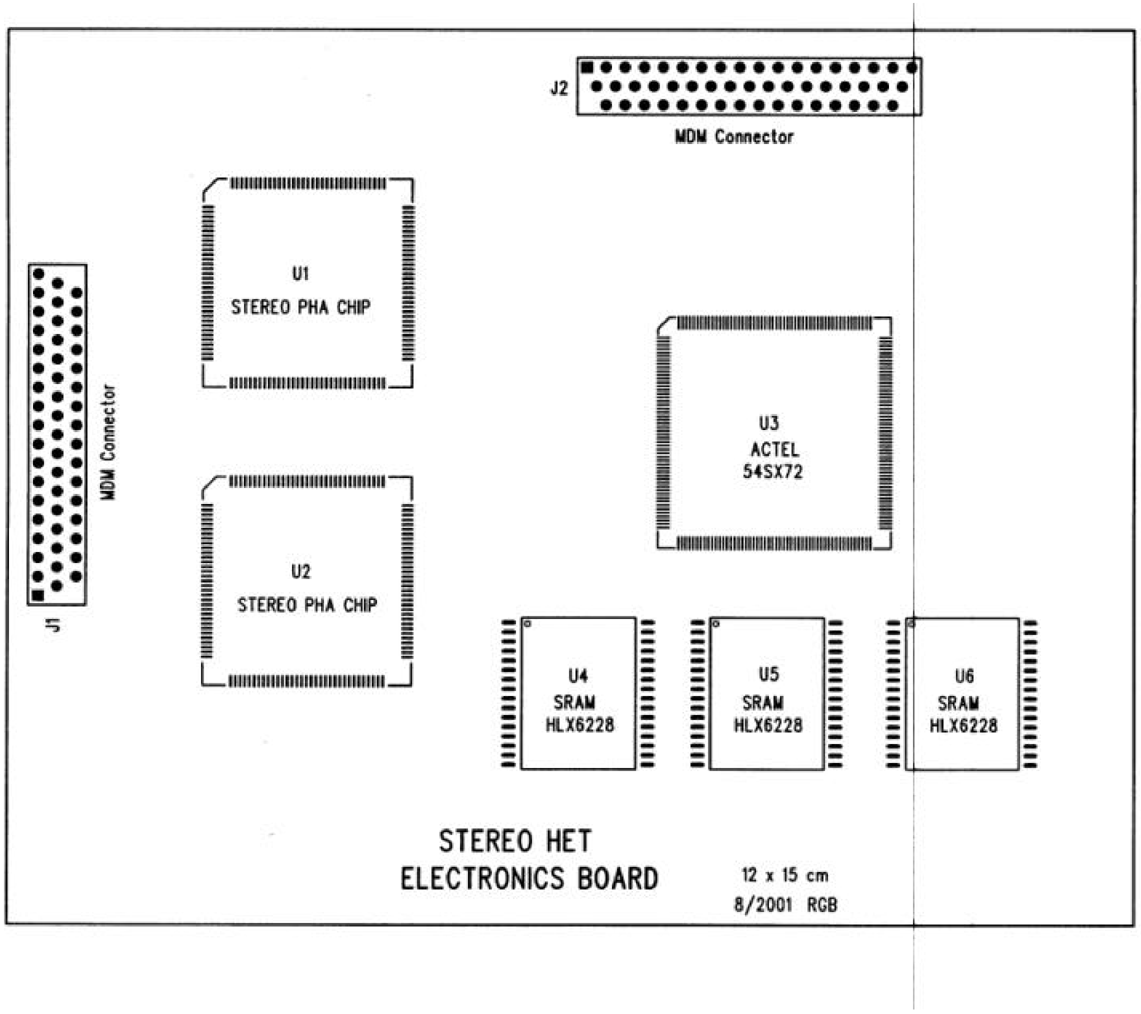
!H1i · H1o · H2

H1o LLD is raised when rates are high so only Z > 2 can trigger

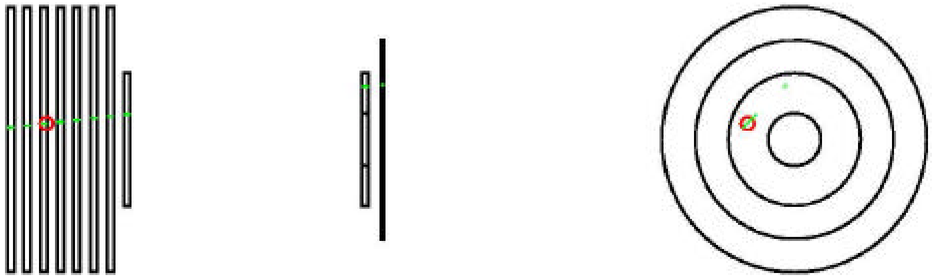
HET Front-End Processing

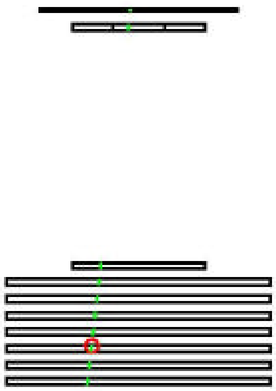


HET Electronics Board Layout



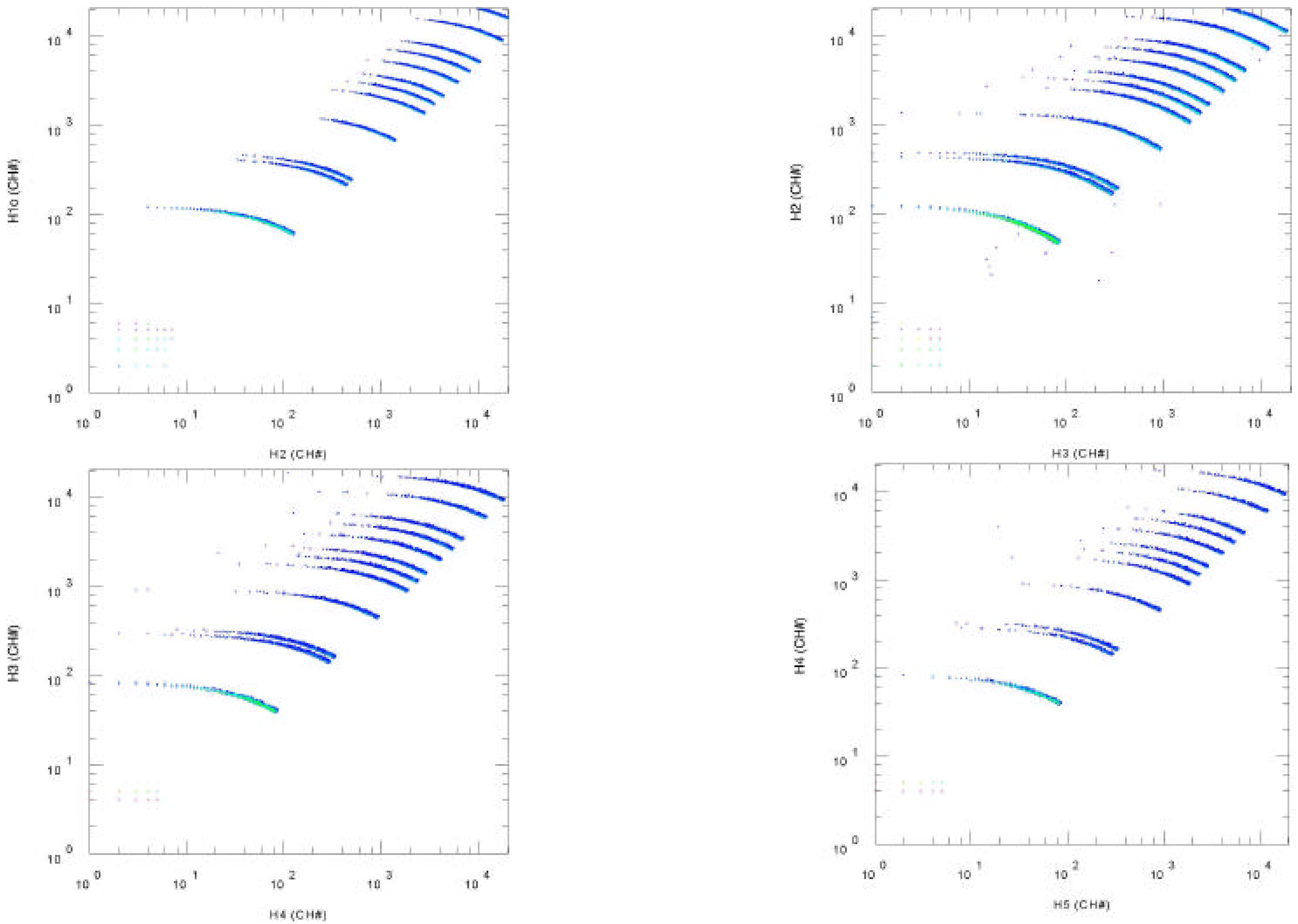
HET Simulations



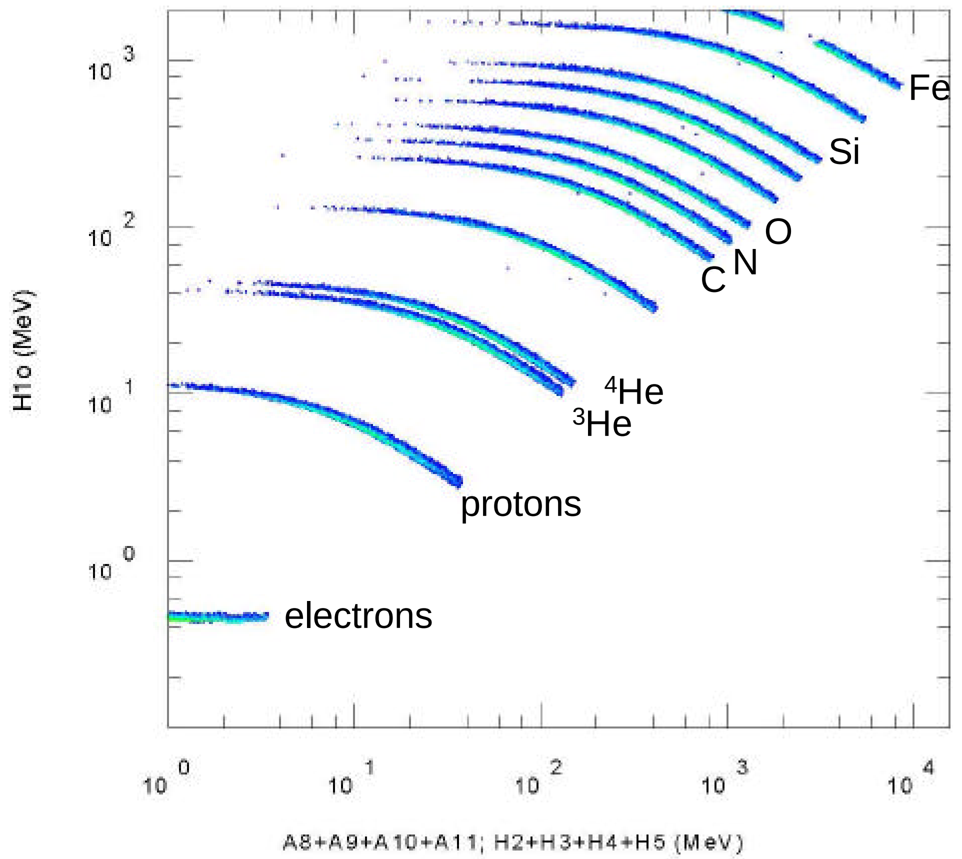


Particle= 5, Z= 2, A= 4, KE= 34.5 MeV/n
theta= 9.3 degrees
phi= 134.7 degrees
xa=-0.79 cm, ya=-0.16 cm, za= 0.00 cm
xb=-0.39 cm, yb=-0.57 cm, zb=-3.50 cm
Stops in H5a: xs=-0.24 cm, ys=-0.71 cm, zs=-4.76 cm

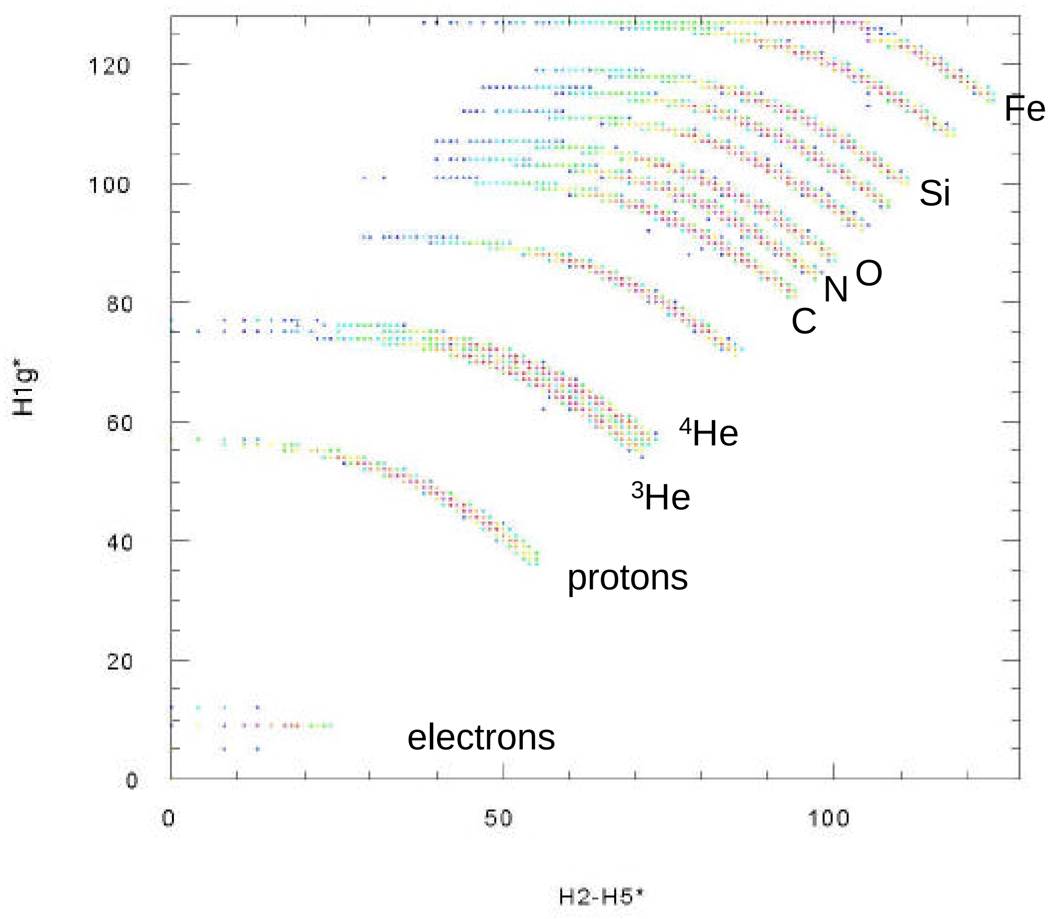
HET Response



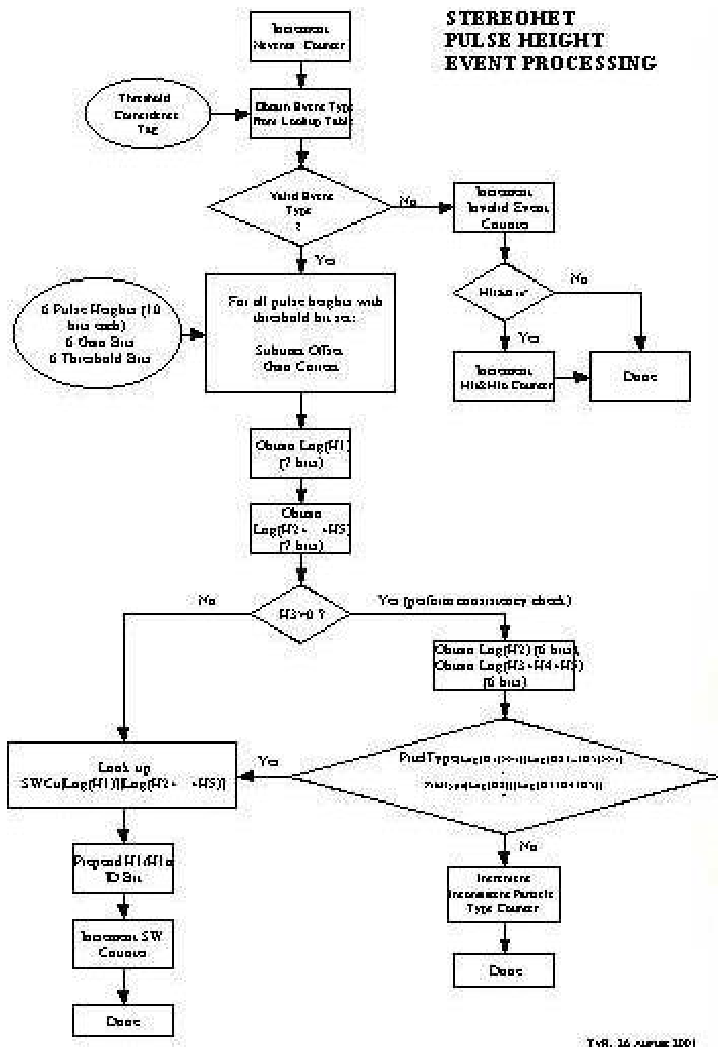
HET Composite Response



HET Composite Log Response



HET On-Board Pulse Height Processing



HET On-Board Code Snippets - I

```
// Code to Create On-board Table for Obtaining DeltaE Log Channel…only the table and bDeltaE are on-board
#define TBLSZ   512
double log2(double x){
                return log(x)/log(2.);
}
int roundoff(double x){
   if(x>0.0)
      return (int)(x+0.5);
  else
      return (int)(x-0.5);
}
// Initialize Look-up Table:
CDeltaE=roundoff(4.*Nlogchs/log2(DeltaEmax/DeltaEmin));
bDeltaE=roundoff(-4.*Nlogchs*log2(DeltaEphmin)/log2(DeltaEmax/DeltaEmin));
TableCDeltaElog2[0]=0;
for(i=1;i<TBLSZ;i++)
    TableCDeltaElog2[i]=roundoff((double)CDeltaE*log2((double)i));
```

HET On-Board Code Snippets - II

```
// On-Board

int CDeltaElog2(int ph)     // note: ph is the ph one would have obtained if the entire dynamic range
                            //        were covered by a single PHA with gain equal to the high gain
{
        int n=0;
        while(ph>TBLSZ-1)   // need to hardcode TBLSZ-1 on-board to avoid repeated subtraction of 1
        {
            ph>>=1;
            n+=CDeltaE;
        }
        return (TableCDeltaElog2[ph]+n);
}

// log compressed DeltaE channel by table lookup = (CDeltaElog2(DeltaEph)+bDeltaE)>>2
```

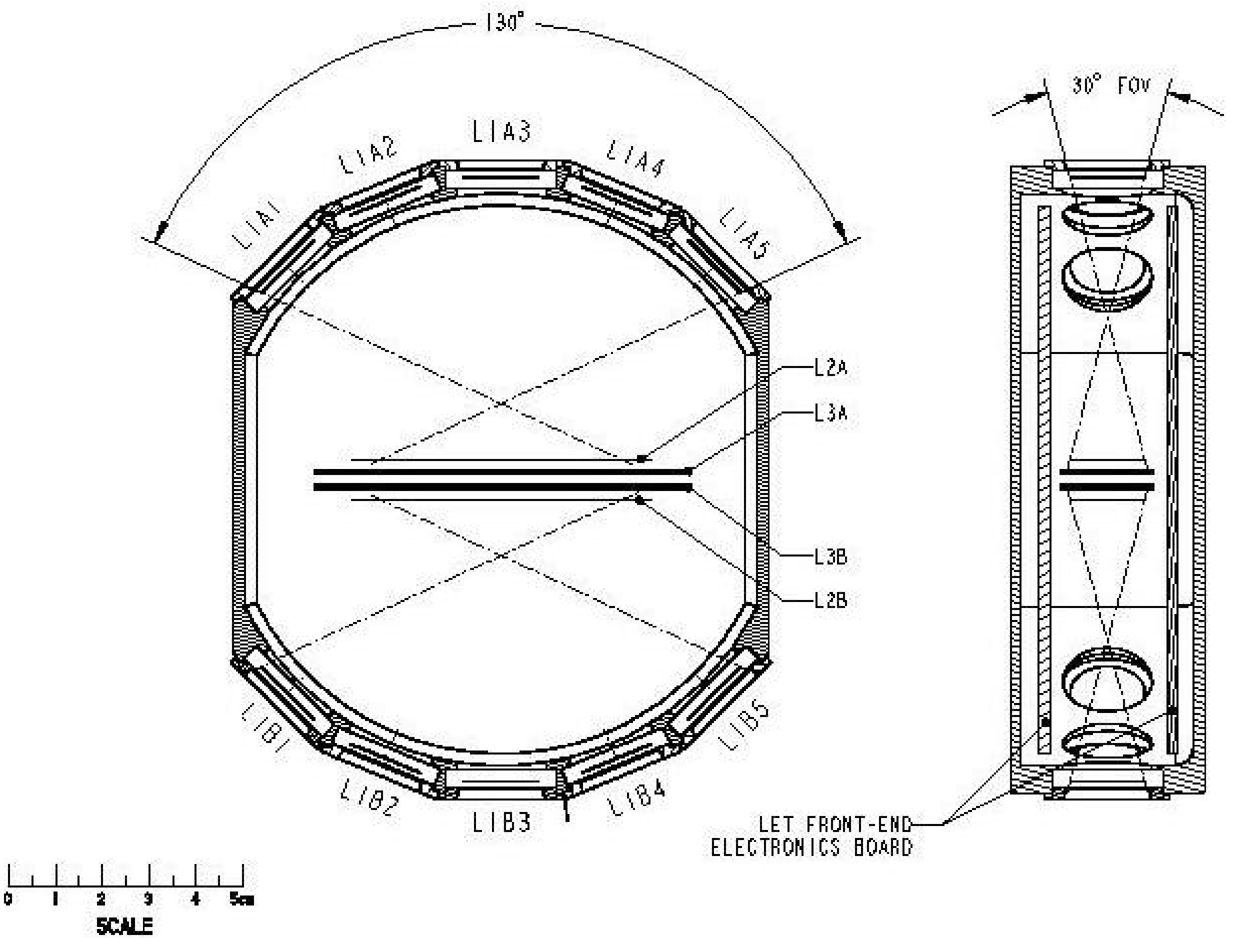
HET On-Board Code Snippets - III

```
/* 32-bit -> 16-bit compression for SW and HW rates     */
/* useage:  rateout=pack_rate(ratein);  */
unsigned int pack_rate(long ratein)
{
        unsigned int rateout, power=0;
        while (ratein&0xfffff000)
        {
                power+=0x0800;
                ratein>>=1;
        }
        rateout=ratein;
        if (power)
                rateout=power+0x0800|((rateout&0x07ff));
        return rateout;
}
```

Low Energy Telescope (LET)

Caltech/JPL/GSFC

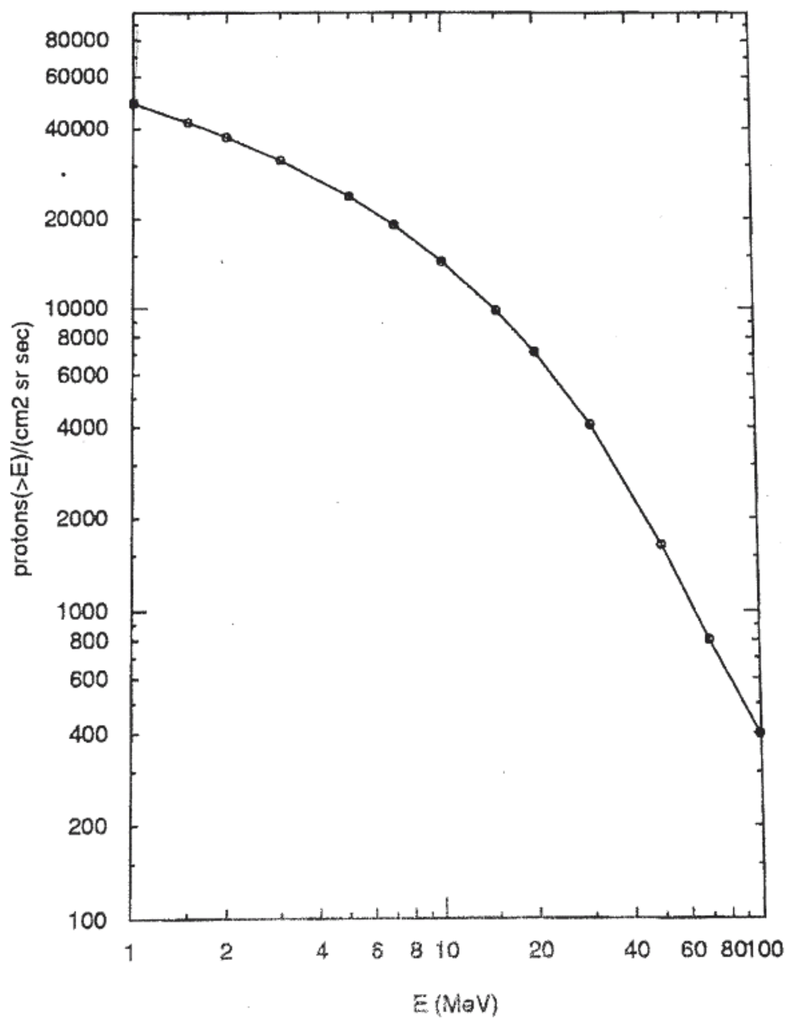
Low Energy Telescope (LET) Schematic



LET Performance Requirements

Description	Goal	Requirement
FOV	2 oppositely directed 130 x 30 degree fans	2 oppositely directed 100 x 30 degree fans
Energy Range (MeV/nucleon)	H: 1.4 - 6 He: 1.4 - 13 O: 2.5 – 25 Fe: 2.5 - 50	H: 1.5 - 3 He: 1.5 - 13 O: 3 – 25 Fe: 3 - 25
Geometric Factor cm^2 ster	H, He: 0.9 $5<Z<27$: 4.5	H, He: 0.5 $5<Z<27$: 2
Element Resolution	Also resolve Na, Al, S, Ar, Ca	Resolve H, He, C, N, O, Ne, Mg, Si, Fe
^{4}He Mass Resolution	<0.25 AMU	<0.35 AMU
Max Event Rate	5000 events/sec	1000 events/sec
Energy Binning	8 intervals per species for $Z>1$ 4 intervals for H	6 intervals per species for $Z>1$ 3 intervals for H
Species Binning	Add S, Ar, Ca	H, ^{3}He, ^{4}He, C, N, O, Ne, Mg, Si, Fe
Time Resolution	1 minute H, He, 15 minutes $Z>5$ 4 prioritized events/sec	15 minutes 1 prioritized event/sec
Beacon Telemetry:	1 minute for H, He, $5<Z<27$	1 minute for H, He, $5<Z<27$

Bastille Day Event Proton Spectrum



Compiled by
Allan Tylka, NRL

LET Detector Table

LET Silicon Detectors

Detector ID[1]	Thickness (μm)	Active Area (cm^2)	Number of Devices	Segments per Device	Min. Energy to Penetrate[2] (MeV/nuc) H & ^{4}He	O	Fe
L1A	20	2.0	5	3	1.3	2.3	2.8
L2A	50	10.24	1	10	2.6	5.3	7.8
L3A	1000	15.6	1	2	12.7	27.5	49.0

1) detectors are identical for B-end of LET

2) assumes 8 μm kapton window in front of L1

LET Thresholds and Gains

HET Thresholds and Gains 8.30.01

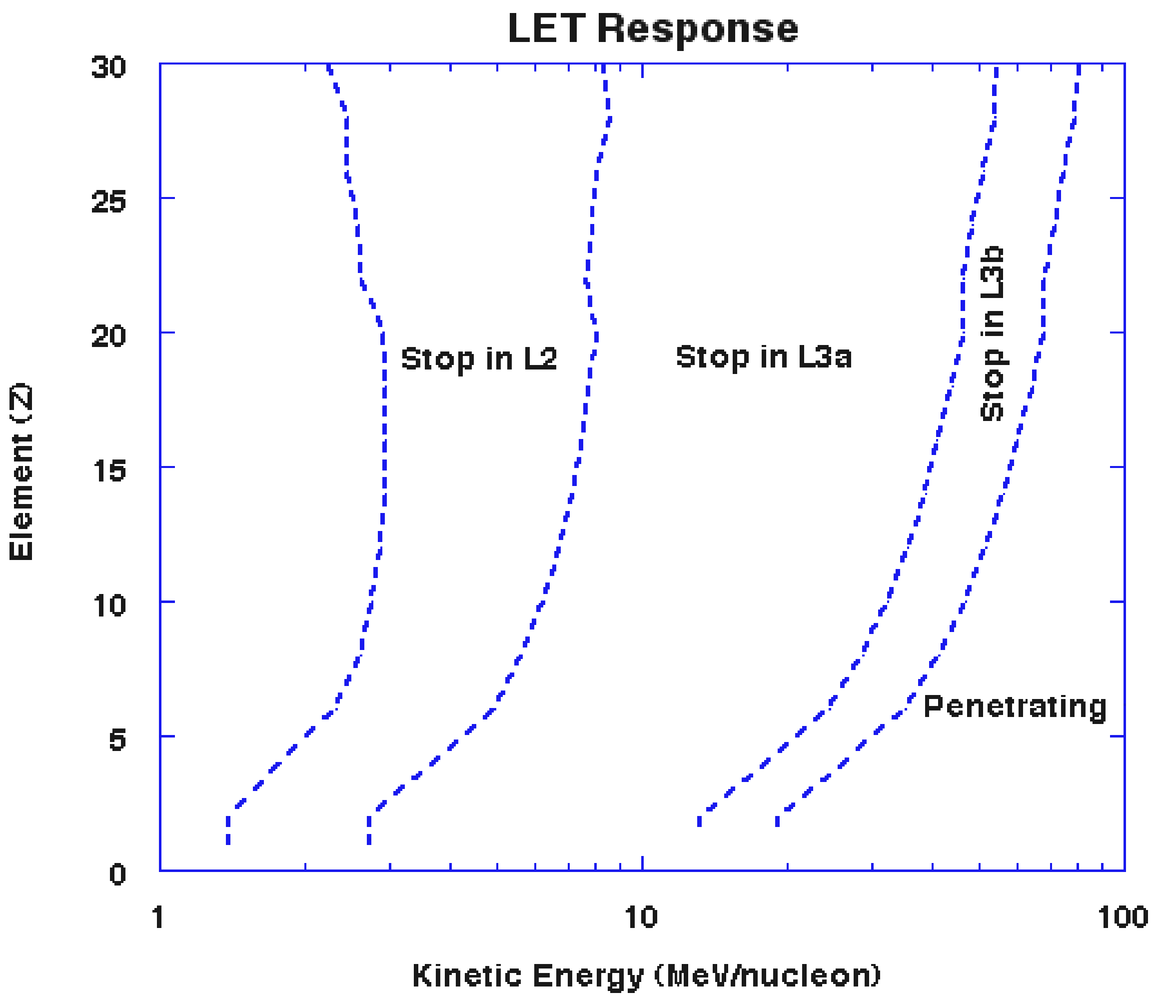
Detector	Area cm2	Thick (micron)	Detect. Cap. (pf)	Est. (1) Noise (MeV)	Minimum Thresh (MeV) (=5 x n)	Nominal Hi-gain Thresh (MeV)	Min. Hi-gain Setting (MeV)	Hi-gain Full Scale (MeV)	Hi-gain channel width (MeV)	Delta (2) Threshold Adjust. (MeV)	Max. Hi-gain Thresh (MeV)	Min. Lo-gain Thresh (MeV)	Delta (2) Adjust. (MeV)	Nom (3) Hi-Rate Thresh (MeV)	Lo-gain Full Scale (4) (MeV)	Lo-gain channel width (MeV)	Total Dynamic Range (5)
H1i	0.5	1000	6	0.037	0.185	0.20	0.1841	92	0.045	0.006	5.84	3.68	0.09	0.20	1841	0.899	9951
H1o	2.64	1000	30	0.037	0.185	0.20	0.1841	92	0.045	0.006	5.84	3.68	0.09	16	1841	0.899	9951
H2	3.14	1000	36	0.037	0.185	0.20	0.1841	92	0.045	0.006	5.84	3.68	0.09	0.20	1841	0.899	9951
H3,H4,H5	12	2000	273	0.080	0.400	0.45	0.3989	199	0.097	0.012	12.65	7.98	0.19	0.45	3989	1.948	9973
H6	12	1000	137	0.037	0.185	0.20	0.1841	92	0.045	0.006	5.84	3.68	0.09	0.20	1841	0.899	9951

The maximum H1, H2 energy-loss to meet the science requirements is ~75 MeV; the maximum of interest is ~3000 MeV

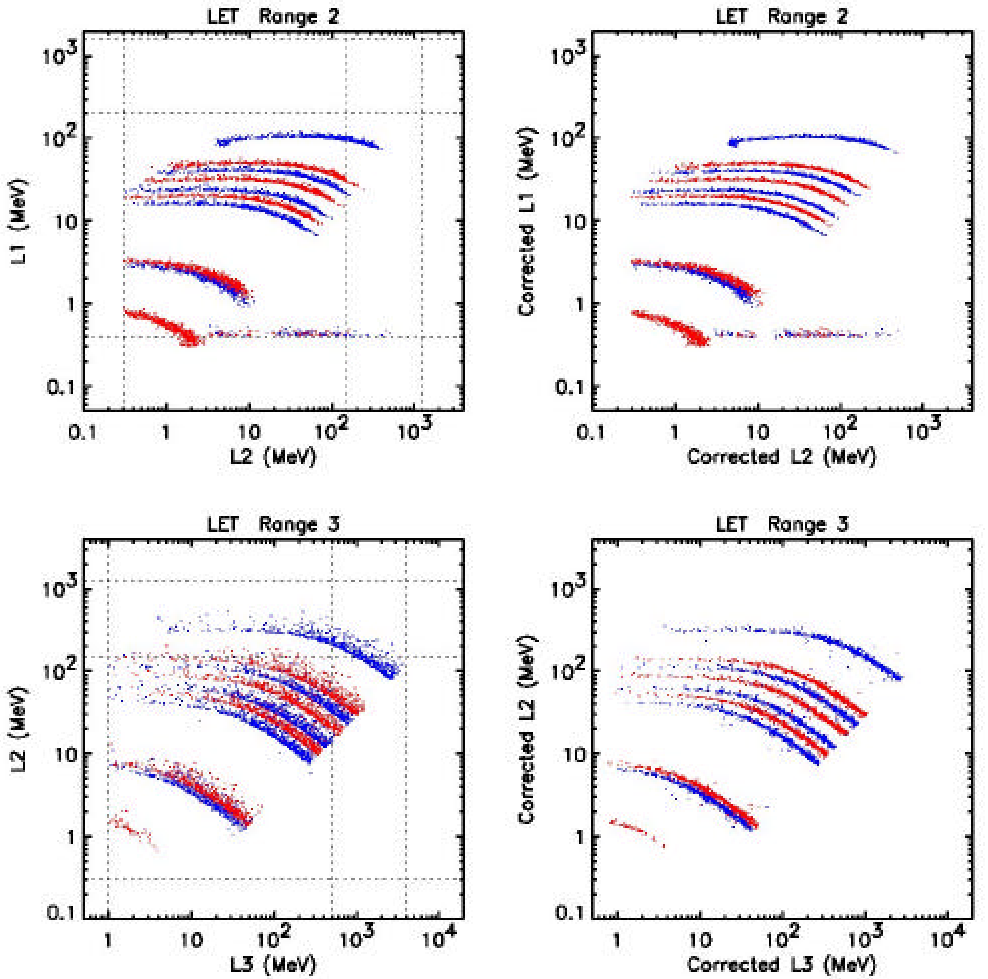
The maximum H3, H4, H5 energy-loss to meet the science requirements is ~100 MeV; the maximum of interest is ~4000 MeV

Notes:
(1) Noise estimated by W. R. Cook, taking into account all known contributions
(2) Nominal thresholds can be adjusted (by command) to accommodate range of thicknesses and noise
(3) For some L1i and L2, and for L1o, L3o, and H1o the low-gain thresholds will be raised during very high-rate periods
(4) Dynamic range = 500 for both low and high gain; nominal high/low gain factor = 20
(5) Ratio of Lo-gain full scale to minimum hi-gain threshold (5 times noise)

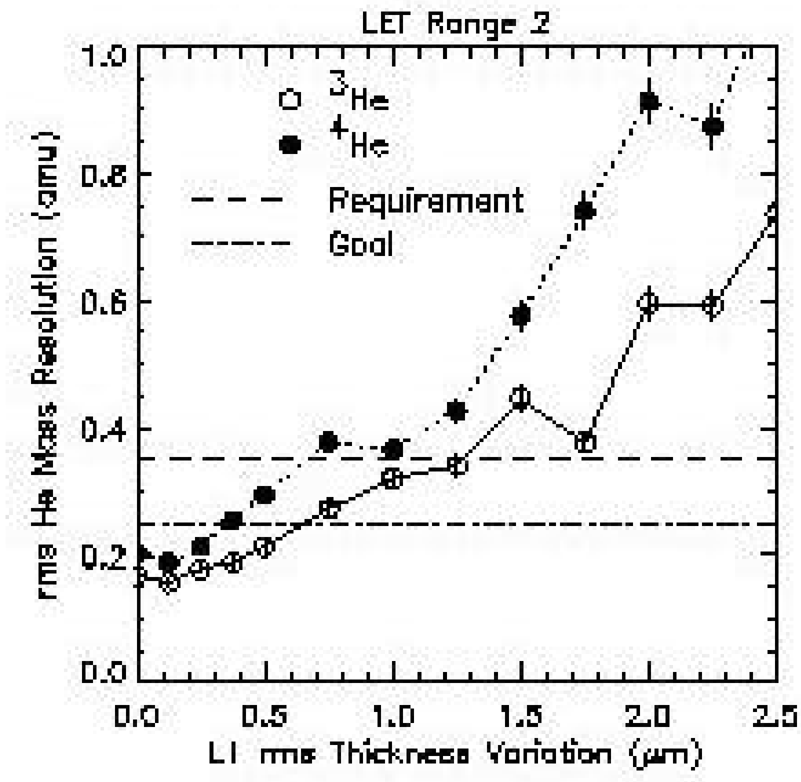
LET Energy/Particle Response

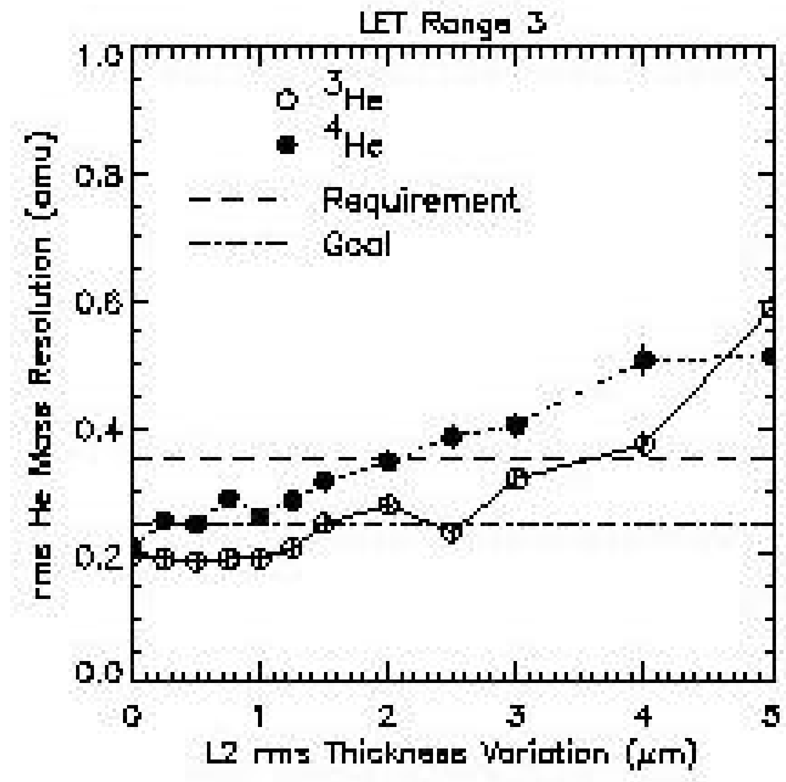


LET dE/dx x E Response



He Isotope Resolution





LET Operation During High-Rate Periods

Requirement: Provide composition and energy spectra measurements over conditions ranging from quiet-time to the largest solar events

Issue: During very high-rate periods (e.g., peak of Bastille Day 2000 event) the single-detector count rates, especially on the front detectors, can exceed 1,000,000/sec, mostly due to out-of-geometry, wide angle protons

Approach:

- L1 detectors are segmented into 3 segments including a small central segment
- Collimation of L1 detectors to shield against wide-angle protons
- Shield sides of telescope to reduce L2, L3 count rates
- Adjust thresholds on selected detectors to reduce overall count rates while maintaining energy and species coverage

LET Operation During High-Rate Periods … Cont

- Thresholds adjusted by ignoring high-gain response on selected detectors
- Adjustments controlled on-board by "OR" of count-rates from detectors that are not adjusted (L1A3, L1B3, L2A5, L2A6, L2B5, L2B6, L3Ai, and L3Bi)

Implementation (in order of occurrence):

- All L1o thresholds raised from 0.7 to 3 MeV
  (reduce H, He geometry by x5 and singles by x5)
- Raise all but L2A5,6, L2B5,6 thresholds from 0.3 to 4 MeV
  Raise L3Ao, L3Bo thresholds from 1 to 20 MeV
  (reduce H, He geometry by additional ~x5 factor)
- Raise all L1i thresholds except L1A3, L1B3 from 0.3 to 3 MeV
  (reduces H, He geometry & singles by additional ~x5 factor)

LET Operation During High-Rate Periods … Cont

Considerations:

- To a large extent, full geometry for Z = 6 particles is maintained
- H and He coverage maintained with adequate geometry
  along with front/back response
- At most two thresholds used for a given detector
- Requirements for adjustments must employ hysteresis and suitable time average
- Simulations based on Wind/ACE events needed to test approach
- Test in laboratory by reducing nominal, high-gain thresholds

STEREO/IMPACT
HET/LET
Solid-State Detectors

Caltech / JPL / GSFC

M. Wiedenbeck JPL

Overview

- Ion-implanted silicon solid state detectors are used as the sensor elements in the IMPACT HET and LET Instruments
- A total of 5 different detector designs are required:
  - One design for HET H1 and H2 detectors, designated "H1"
  - One design for HET H3–H6, designated "H3"
  - One design each for LET L1, L2, and L3
- The H1, H3, L2, and L3 designs are relatively routine and do not push the state of the art. Characteristics are summarized on the next page.
- The L1 design is somewhat challenging because these detectors are thin ($\sim 20\ \mu$m) and good thickness uniformity is desired. Details of the L1 development status are given later in this presentation.

H1, H3, L2, L3 Detector Specification Summary

1	Detector Identification	L2	L3	H1	H3
2	Shape	Rectangular	Rectangular	Circular	Circular
3	Active Area Dimensions (cm)	6.4×1.6	7.8×2.0	2.0 diameter	4.0 diameter
4	Overall Area Dimensions (cm)	6.8×2.0	8.2×2.4	2.4 diameter	4.4 diameter
5	Average Thickness (μm)	50 ± 5	1000 ± 50	1000 ± 50	1000 ± 50
6	Max. Thickness Nonuniformity (μm)	5	25	25	25
7	Offcut Min. Dimensions (cm) *	2 each @ 6.4×0.3 2 each @ 1.6×0.3	2 each @ 7.8×0.3 2 each @ 2.0×0.3	4 each @ 1.0×0.3	4 each @ 1.0×0.3
8	Active Junction-Surface Contacts	10	3	2	1
9	Geometry of Junction-Surface Contacts †	linear array of 10 contacts, each 0.64 cm $\times$ 1.6 cm	linear array of 3 contacts, center contact 2.4 cm long and outer contacts each 2.7 cm long	central circular contact with 0.8 cm diameter surrounded by annular contact with 2.0 cm outside diameter ‡	single circular contact with 4.0 cm diameter
10	Contact Spacing (μm)	20 ± 5	40 ± 10	40 ± 10	40 ± 10
11	Junction Surface Connections	wire bonds	wire bonds	wire bonds	conductive epoxy
12	Ohmic Surface Connections	wire bonds	wire bonds	conductive epoxy	conductive epoxy
13	Max. Depletion Voltage (Volts)	20	200	200	200
14	Min. Breakdown Voltage (Volts)	50	250	250	250
15	Max. Leakage Current (μA)	0.5	2.	1.	1.
16	Max. Alpha Resolution (keV FWHM)	100	100	100	100

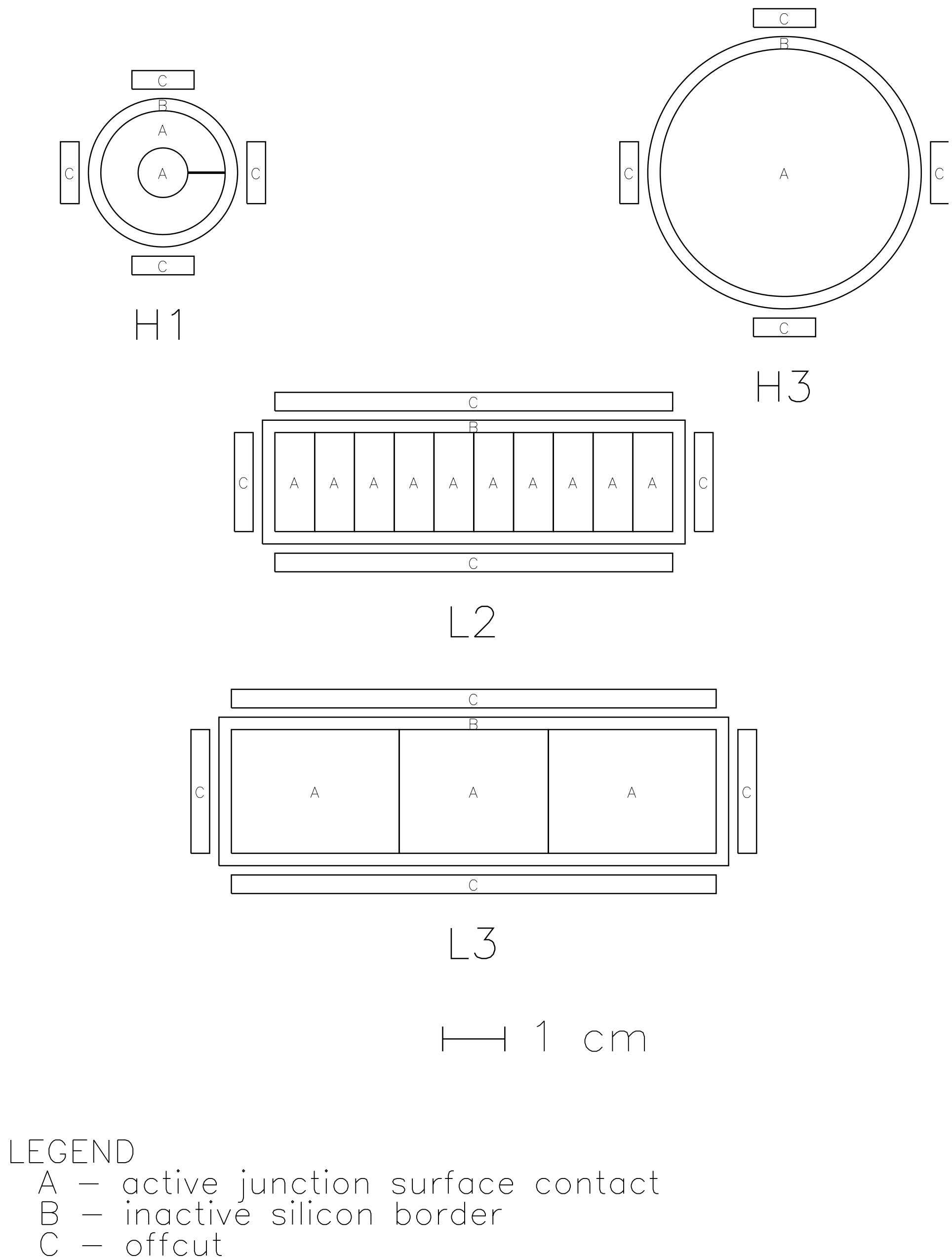
Notes:

* The number and size of offcuts are to be treated as goals.

† In the multi-contact designs, contact dimensions given include the metallization area plus half the gaps between adjacent contacts.

‡ In the H1 design, the annular contact is split so that a narrow lead can be brought out from the central contact to the edge of the active area.

H1, H3, L2, L3 Detector Geometry

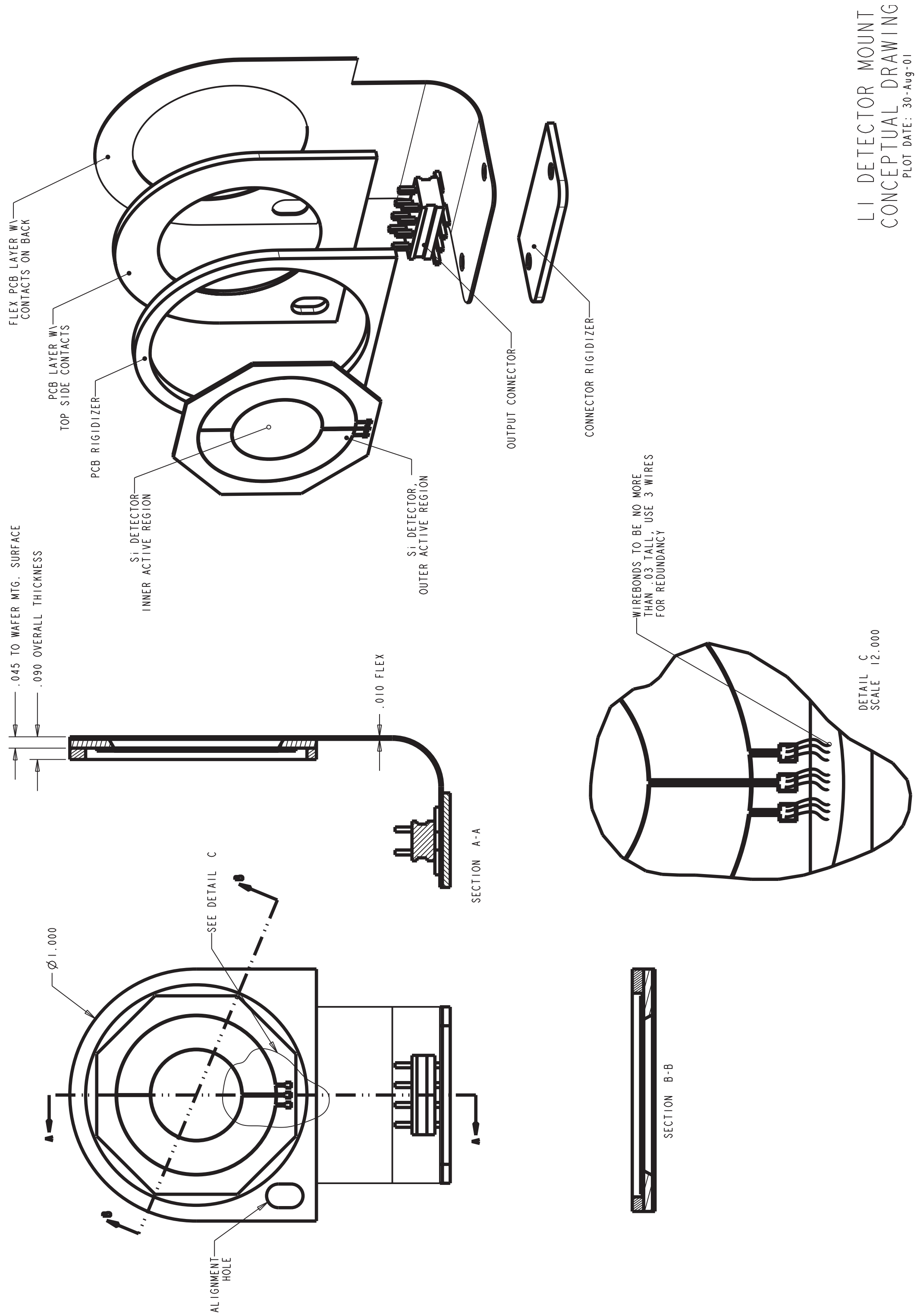


H1, H3, L2, L3 Development Status

- Draft detector specification (version 1.00) has been agreed to by HET/LET team and detector manufacturer, Micron Semiconductor Ltd. of Lancing, Sussex, England.
- Orders for prototype detectors have been placed.
- Micron has designed mask sets required for detector production.
- Mask designs were reviewed in meeting at Micron on 20 August 2001. Minor modifications were agreed to.
- Micron is presently finalizing the mask designs will begin fabrication after approval by the HET/LET team.
- Micron will carry out environmental tests on prototype detectors before delivery. These include random vibration and thermal cycling.
- Delivery of prototype detectors is expected in January 2002.

LET L1 Detectors

- Front LET detectors, designated "L1", need to be thin because the LET threshold corresponds to the energy required to penetrate these detectors.
- Since the IMPACT Phase A report the nominal thickness of the L1 detectors was changed from 15 to 20 μm to increase the signal sizes, reduce capacitance and associated electronic noise, and improve mechanical robustness.
- This L1 thickness, together with the nominal LET window (8 μm of kapton) yields thresholds energies ranging from ~ 1.5 MeV/nuc for He to ~ 3.0 MeV/nuc for Fe.
- The L1 detectors will be segmented into a central region of 0.4 cm^2 area surrounded by a annular region split into two halves each of 0.8 cm^2 area. (The division of the annular region into two halves was introduced subsequent to the IMPACT phase A report to improve noise performance.)
- With these areas the detector capacitance and associated noise will be low enough to allow detection of H using the center segment and to resolve ^{3}He from ^{4}He in all the segments.
- Under high-rate conditions the instrument logic will be able to restrict analysis to particles hitting the center L1 segments, for which the singles rate and associated accidental coincidences will be smallest.

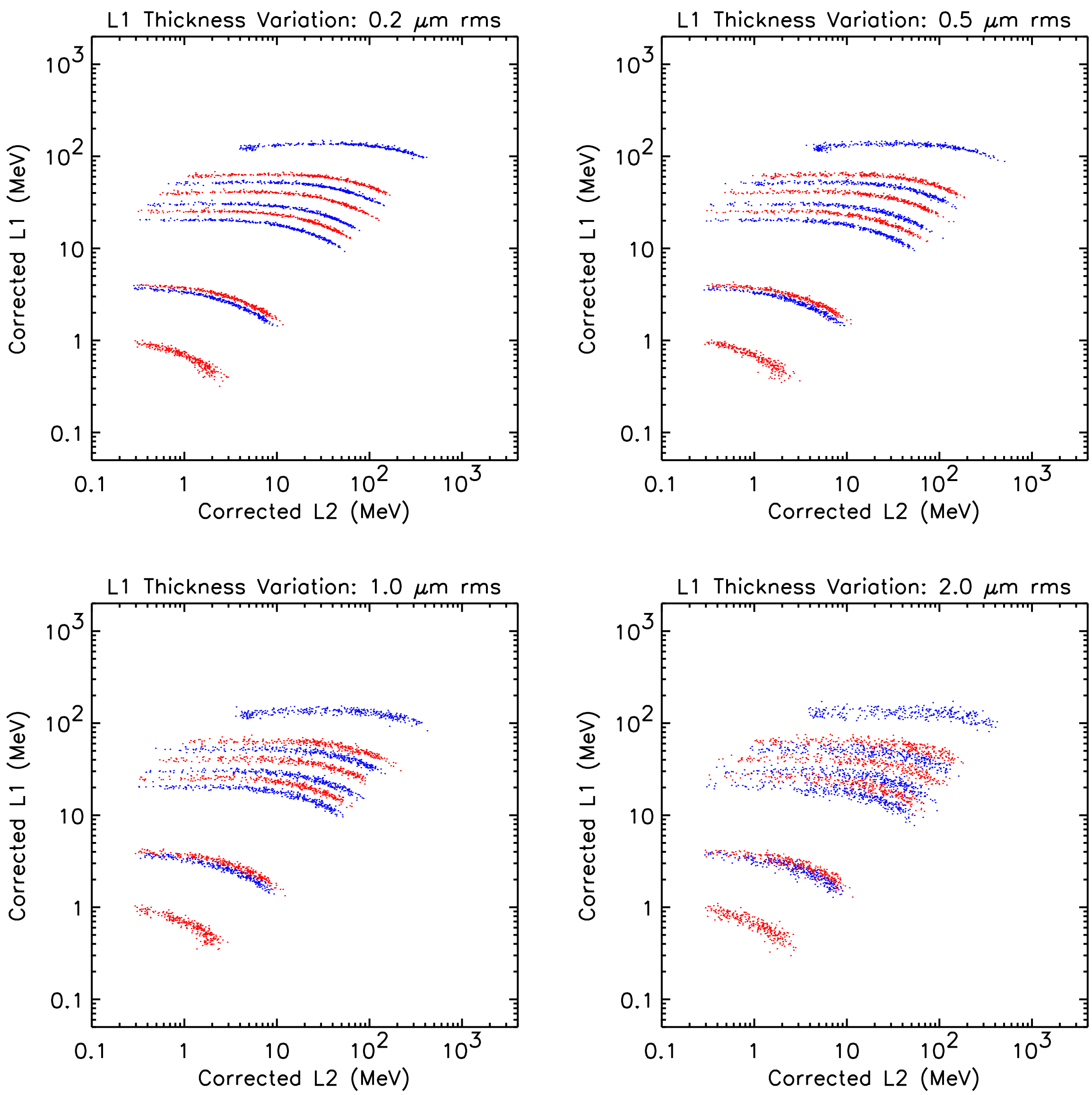

L1 DETECTOR MOUNT
CONCEPTUAL DRAWING
PLOT DATE: 30-Aug-01
FLEX PCB LAYER W\ CONTACTS ON BACK
PCB LAYER W\ TOP SIDE CONTACTS
PCB RIGIDIZER
OUTPUT CONNECTOR
CONNECTOR RIGIDIZER
Si DETECTOR INNER ACTIVE REGION
Si DETECTOR, OUTER ACTIVE REGION
.045 TO WAFER MTG. SURFACE
.090 OVERALL THICKNESS
.010 FLEX
SECTION A-A
WIREBONDS TO BE NO MORE THAN .03 TALL; USE 3 WIRES FOR REDUNDANCY
DETAIL C
SCALE 12.000
Ø1.000
SEE DETAIL C
ALIGNMENT HOLE
SECTION B-B

Thin Si Detectors—Background

- Thin Si detectors ($\lesssim$20 μm) with areas of a few cm^2 have been flown (most notably on Wind/LEMT).
- Thin Si detectors flown to date have been made using surface barrier technology. This technology is sensitive to surface contamination problems and has largely been supplanted by ion-implantation technology which leads to much more robust detectors.
- Si detectors thin enough for STEREO/LET have not been commonly made. For example, the thinnest ion-implanted detectors previously made by Micron Semiconductor were 30 μm thick.
- Good thickness uniformity is needed for the L1 detectors in order to achieve the desired resolution of ion species, and particularly for separating ^{3}He from ^{4}He at low energies where these particles stop in L2. The effect of various amounts of thickness nonuniformity is illustrated in the calculated response matrices shown on the next page.

Monte Carlo Calculation of LET L1 vs. L2 Response

- Calculation includes electronic noise, uncorrectable variation of incidence angle, Landau fluctuations of energy loss, and various assumed amounts of thickness nonuniformity (indicated at the top of each plot).
- Response tracks are shown (bottom to top) for H, ^{3}He, ^{4}He, C, N, O, Ne, Mg, Si, and Fe.



Thin Si Detector Development Project

- JPL / Caltech is presently involved in a technology study related to the development of thin, large-area Si detectors.

- Because of STEREO needs for L1 detectors, some work was started in late 1999 to understand and improve capabilities for making thin detectors of the 2 cm^2 area needed for LET

- Two approaches have been tried:

  A: conventional fabrication from Si wafers (3 inch diameter) lapped and polished to the desired detector thickness

  B: etching of a thicker Si wafers down to the desired thickness over the smaller area needed for the detector

Progress to Date at Micron Semiconductor

- A number of improvements in detector fixturing and processing techniques were developed by Micron Semiconductor to allow successful fabrication of thin detectors.

- Micron has already delivered thin detectors (thickness range: 13 to 24 μm) made with the two techniques. A total of 14 such detectors (4 of type A, 10 of type B) are presently being characterized at Caltech / JPL.

- A photograph of one of these detectors is shown on the next page. This detector is very similar to the planned LET L1 detectors except that

  - the annular region is segmented into 4 rather than 2 contacts

  - the G10 mount and electrical connections are not of the flight design

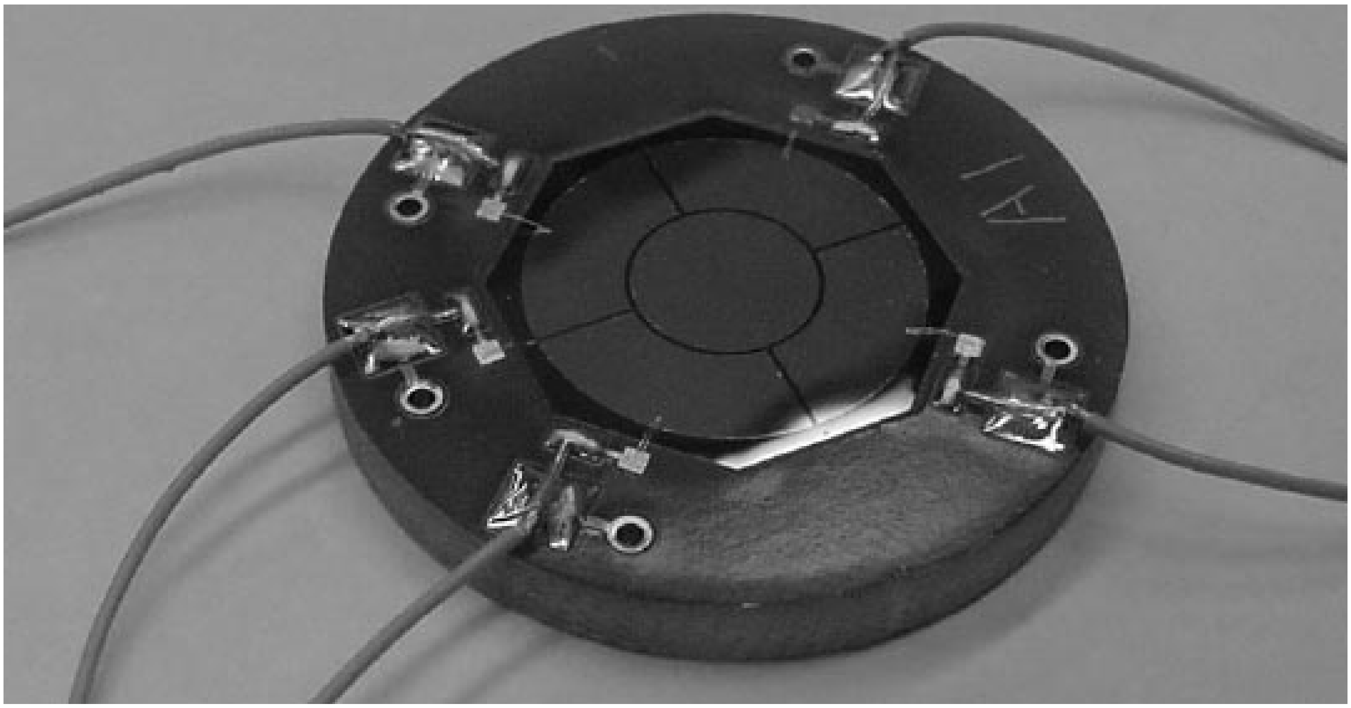
- The following page shows a measured dE/dx vs. E response matrix for alpha particles from a ^{228}Th source penetrating the pre-prototype L1 detector and stopping in a thick detector behind it. The center region of the L1 detector was used to provide the dE/dx signal.

- Even with Micron's process improvements, the yield of detectors produced using method A has been very low.

- The yield of detectors produced using method B has been significantly better. However, most such detectors tested thus far have poor thickness uniformity.

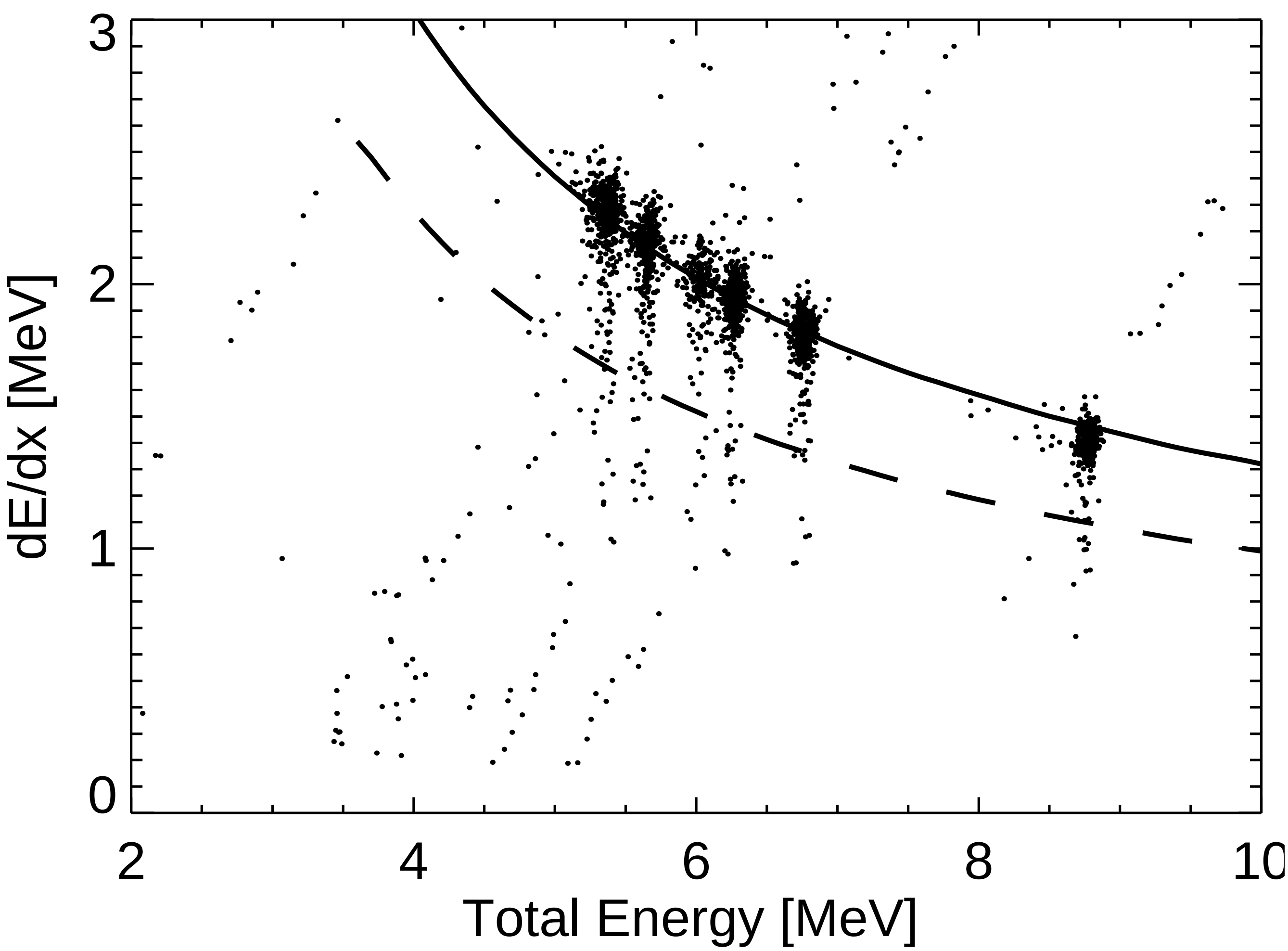
Pre-Prototype L1 Detector from Micron Semiconductor

Active Area: 2 cm^2;   Thickness: 14 μm



dE/dx vs. E Response Matrix

- Central region of L1 detector used for dE/dx measurement
- Stimulus: alpha particles from ^{228}Th source
- Calculated response tracks:
  - solid: ^{4}He
  - dashed: ^{3}He

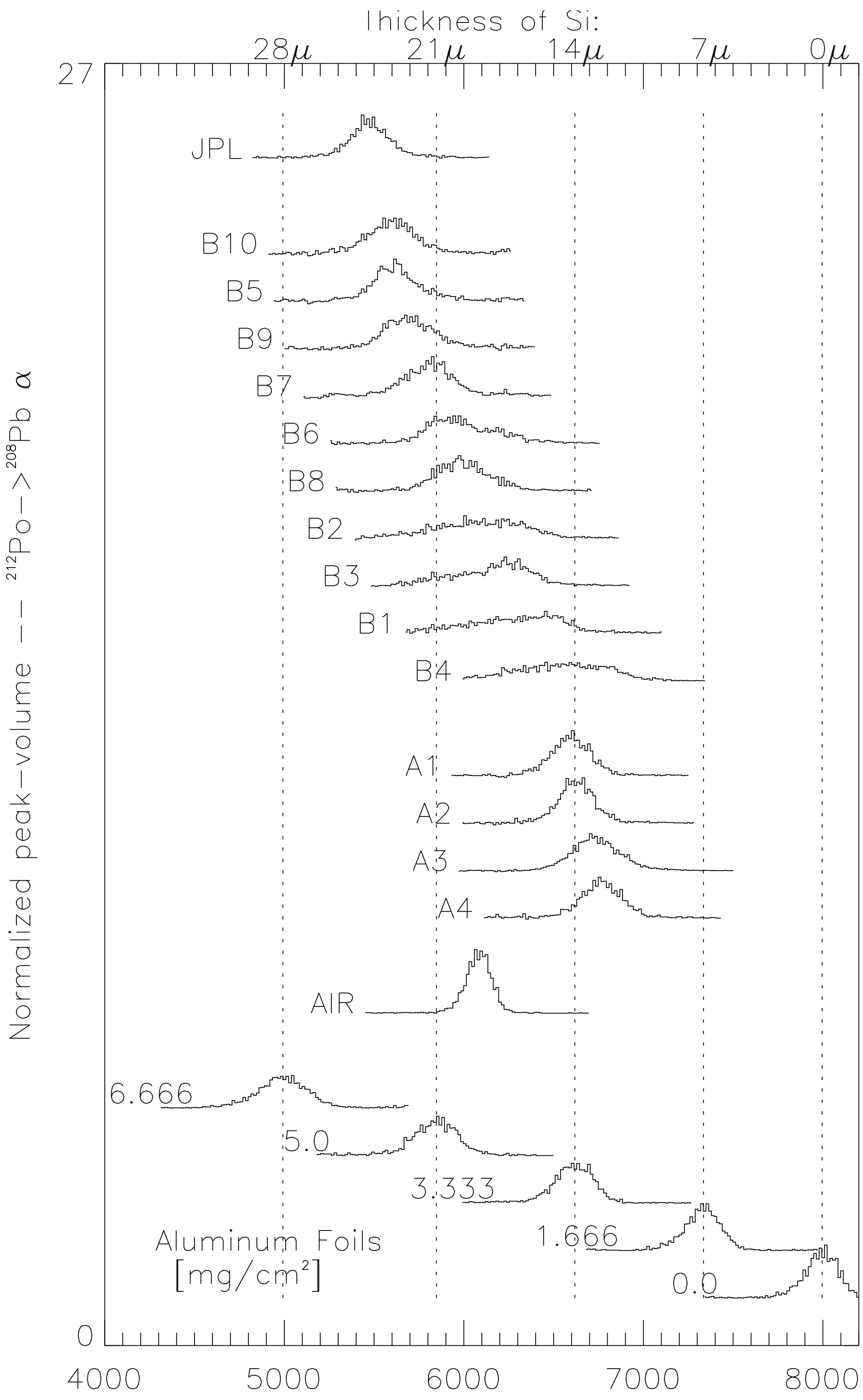


Silicon Thinning by JPL / MDL

- As part of the Thin Silicon technology project, the JPL Micro-Devices Laboratory (MDL) has been working on alternative etching techniques to produce more uniform Si membranes.
- Tests of a first MDL sample at Caltech / JPL indicate that it has much better thickness uniformity than Micron-etched samples.
- Plots on the following page compare pulse height distributions for alpha particles penetrating various thinned samples and detected in a thick Si detector behind them. Samples include:
  - "A" detectors made from 3-inch Si wafers lapped and polished to the desired thickness
  - "B" detectors etched down from 140 μm Si wafer by Micron using TMAH as the etchant.
  - JPL sample etched down from 300 μm Si wafer using KOH as the etchant (not yet processed to make a detector).
  - aluminum foils for calibration of absolute thicknesses.
  - air to give an indication of the peak width without thickness variations.

Thin Sample Characterization with Alpha Particles

Full area of detector exposed to alpha particles.

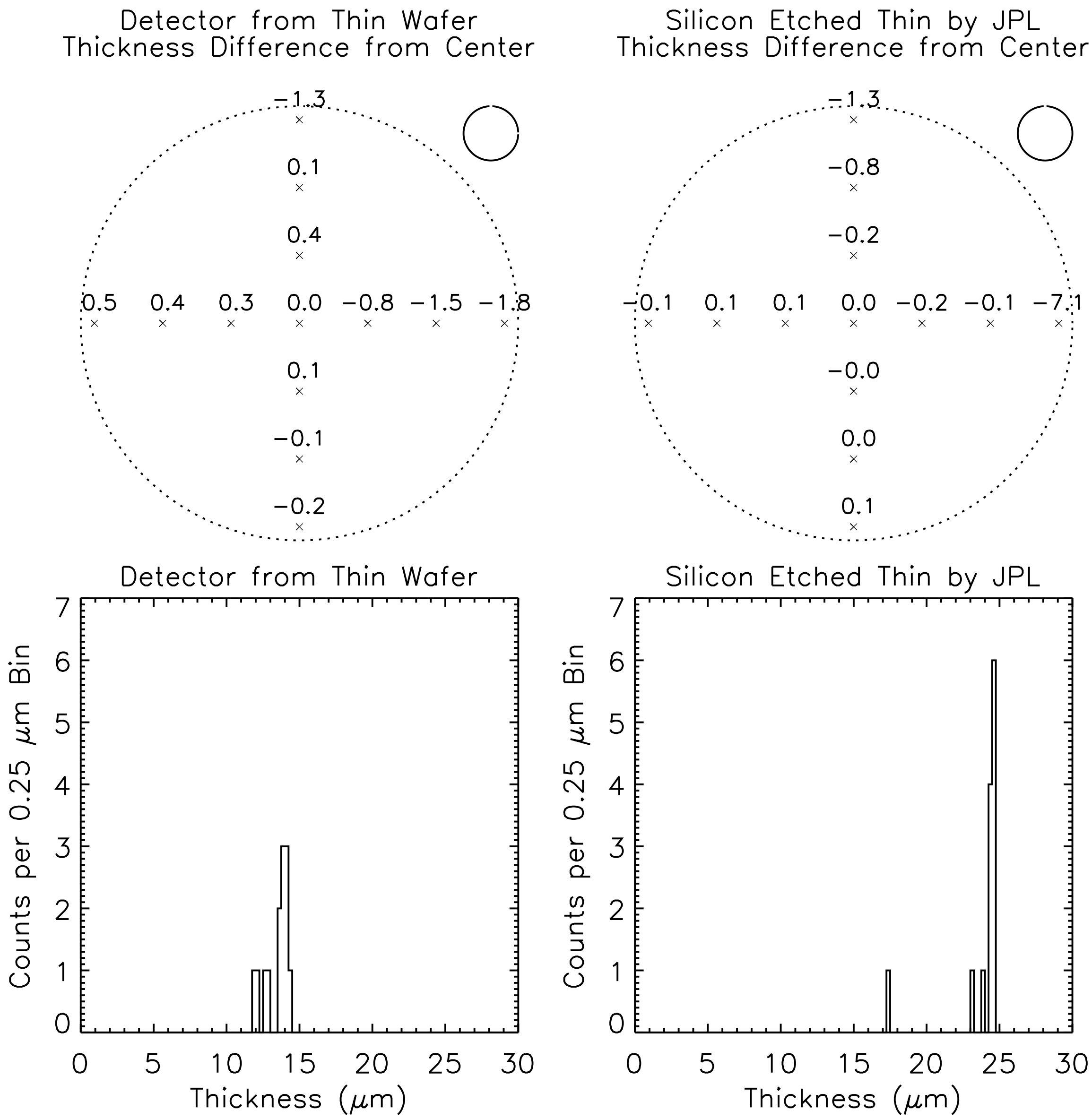


Thickness Maps

- Coarse characterization of detectors using full-area alpha particle exposures is only sensitive to relatively large variations of thickness because peak-broadening effects of these variations are compounded in quadrature with other effects such as Landau fluctuations of energy loss.
- To more precisely characterize thickness variations, diameter scans of detectors were made using alpha particle beams collimated to produce a spot size of ~ 2 mm diameter. Centroids of pulse height distributions accumulated with high statistics give good measures of the thickness variations independent of other peak-broadening effects.
- The plots on the following page compare the thickness variations of a detector (A1) made from a thin wafer (left) with those of the sample thinned using KOH (right). The histograms of the measured thicknesses show the significantly smaller thickness spread of the KOH-thinned sample.

Detailed Thickness Map Comparison

- Maps made using collimated alpha particle source. Small circle at the upper right of the maps shows approximate size of the alpha particle beam hitting the thin detector.



Plan for Fabrication from JPL-thinned Silicon

- Silicon thinning process being used at JPL relies on KOH as the etchant.
- There are issues with processing the KOH-thinned silicon to make detectors:
  - KOH-etched silicon has a rough ("orange peel") surface on small scales. This might interfere with uniform ion implantation.
  - Residual potassium could migrate during high temperature (1100°C) oxidation step, ruin oxides, and contaminate the oven.
- A process for surface-smoothing has been found, involving a brief finishing etch in a gas of XeF_2 + He.
- Micron Semiconductor and JPL / MDL have agreed on a process flow which should avoid problems with potassium contamination:
  1. Micron purchases Si wafers and does front-side processing (which involves high temperature oxide growth)
  2. Micron ships partially-processed wafers to JPL for thinning using KOH etchant. JPL returns thinned wafers to Micron.
  3. Micron completes the back-side processing of the detectors and tests completed devices prior to delivery to Caltech.

Silicon Processing Improvements at JPL

- JPL / MDL has a new technique for achieving the desired absolute thickness:

  1. pre-etch small test areas of thick wafer to depth corresponding to desired thickness (by timing the etch)
  2. etch the entire wafer until test sections just etch through to other surface—silicon remaining in other areas should equal the depth of the pre-etch

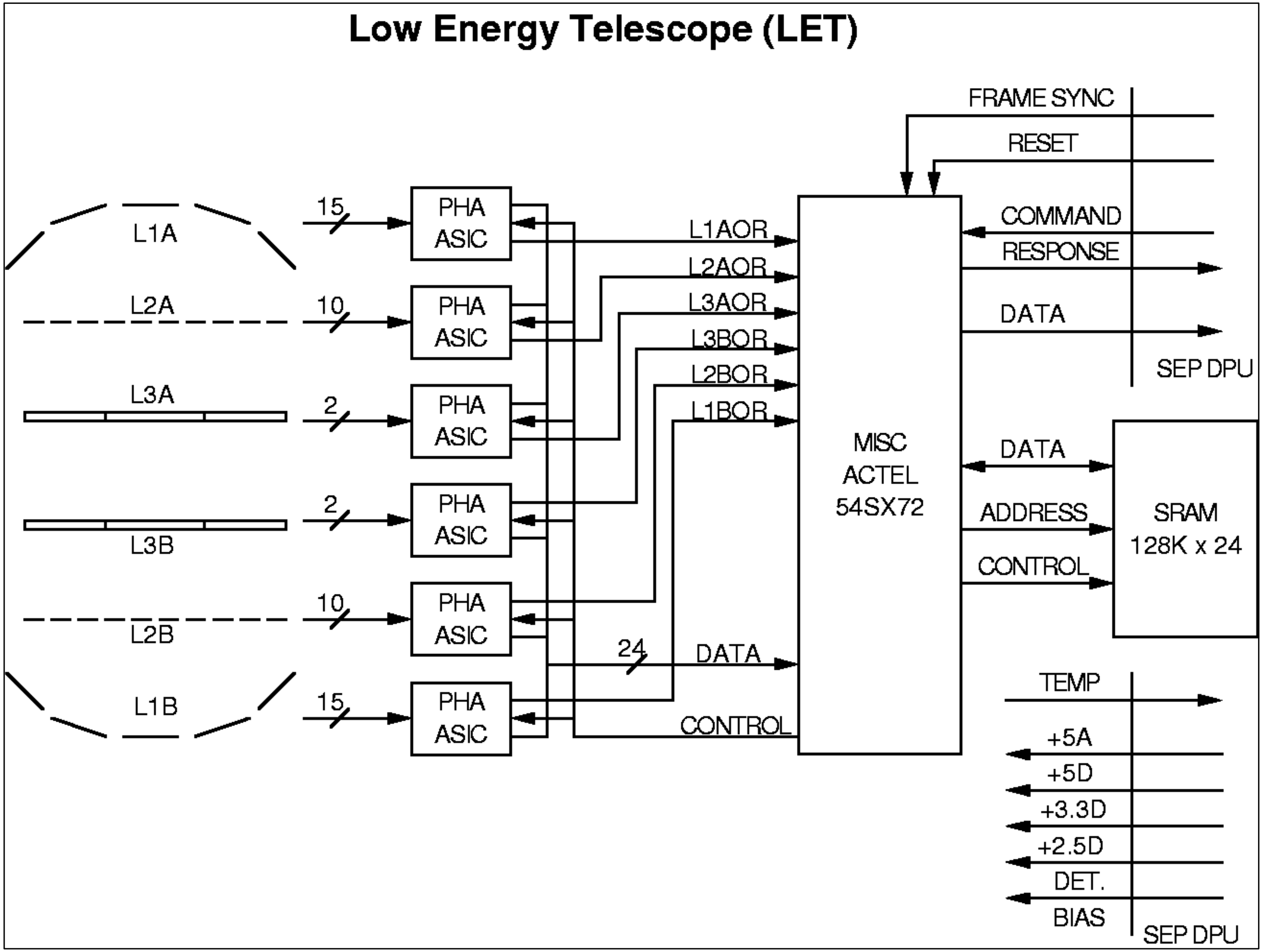
ITAR Clearance

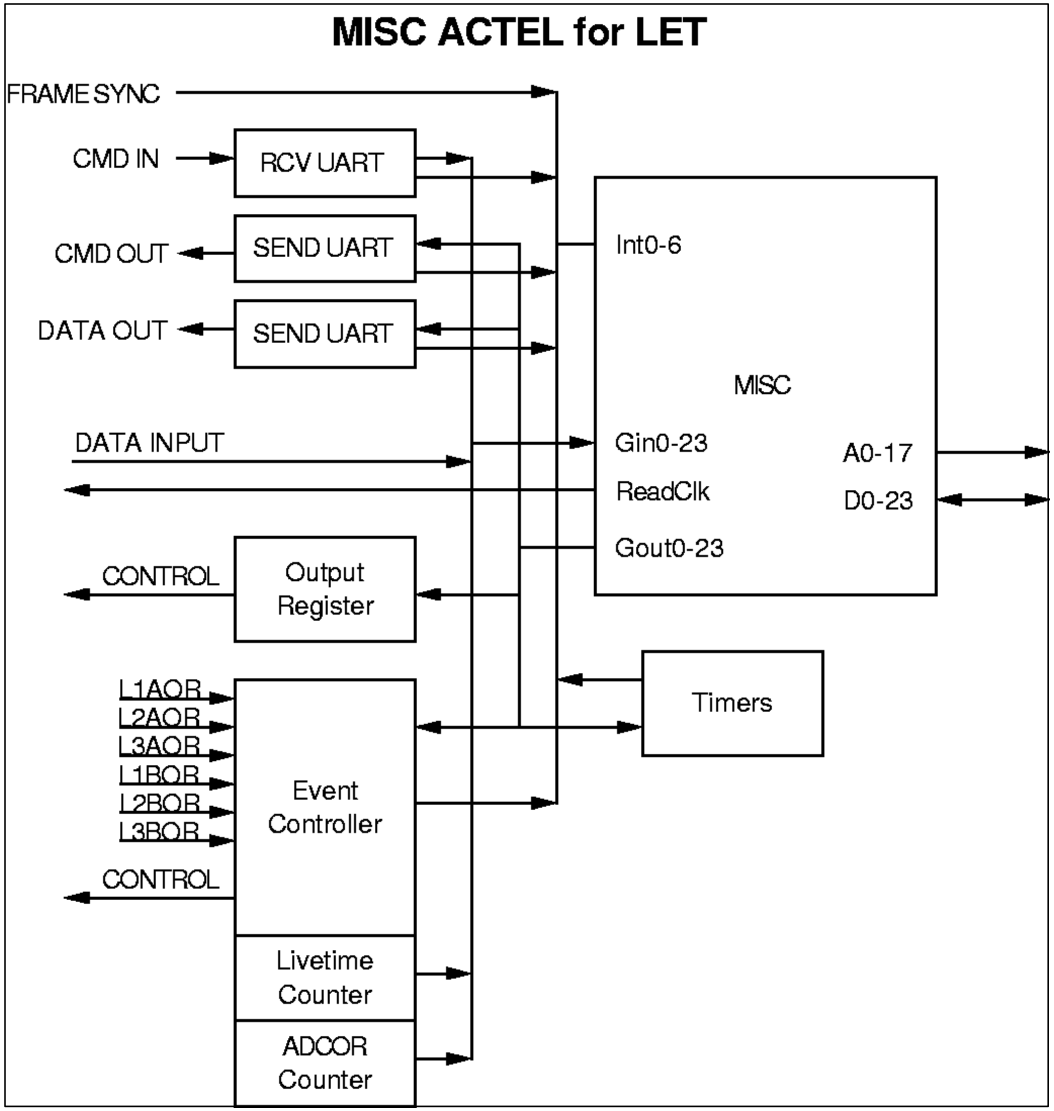
- Planned shipping of partially-processed silicon wafers from JPL to Micron has been reviewed for possible ITAR implications by JPL International Affairs attorneys.
- It has been determined that the planned activity falls under Department of Commerce rules, not ITAR.
- JPL has approved the planned shipments.

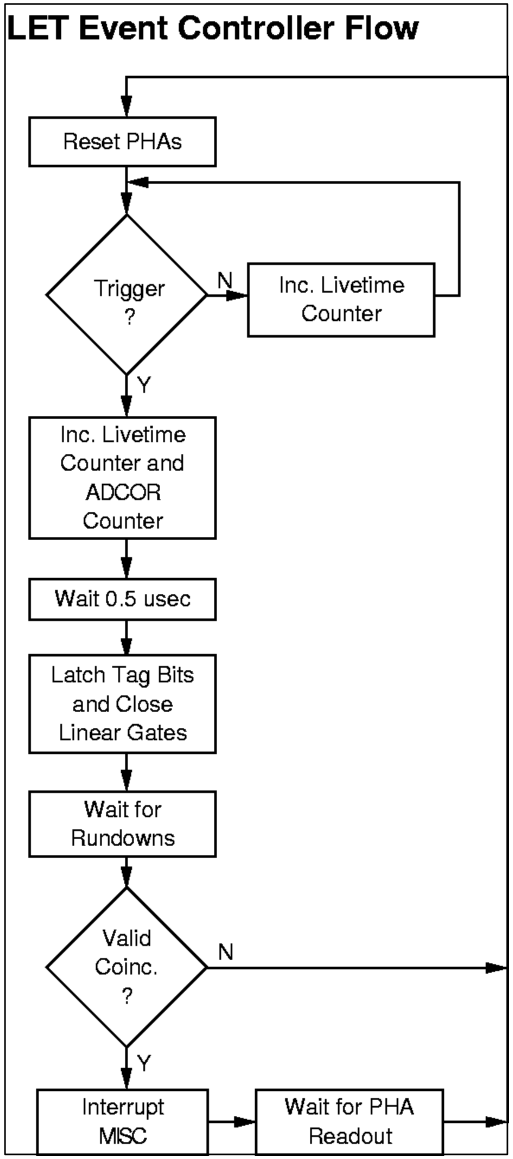
Backup Plans

- If a problem arises in making detectors from JPL-thinned samples, it would be possible to adopt one of the two approaches that has already been used to produce operational thin detectors:
  - Use detectors thinned by Micron using TMAH.
  - Use detectors made from silicon wafers lapped and etched thin.
- Issues:
  - The best detectors made by thinning in TMAH have marginally-acceptable thickness nonuniformity.
  - The most-recently-produced samples were better than earlier samples indicating that further improvement of the thinning process may be possible.
  - Yield was poor for detectors made from thin wafers due to breakage during various steps of the manufacturing process.
  - Increase of thickness from 15 to 20 μm should result in less breakage, but it is not know how significant this improvement will be.

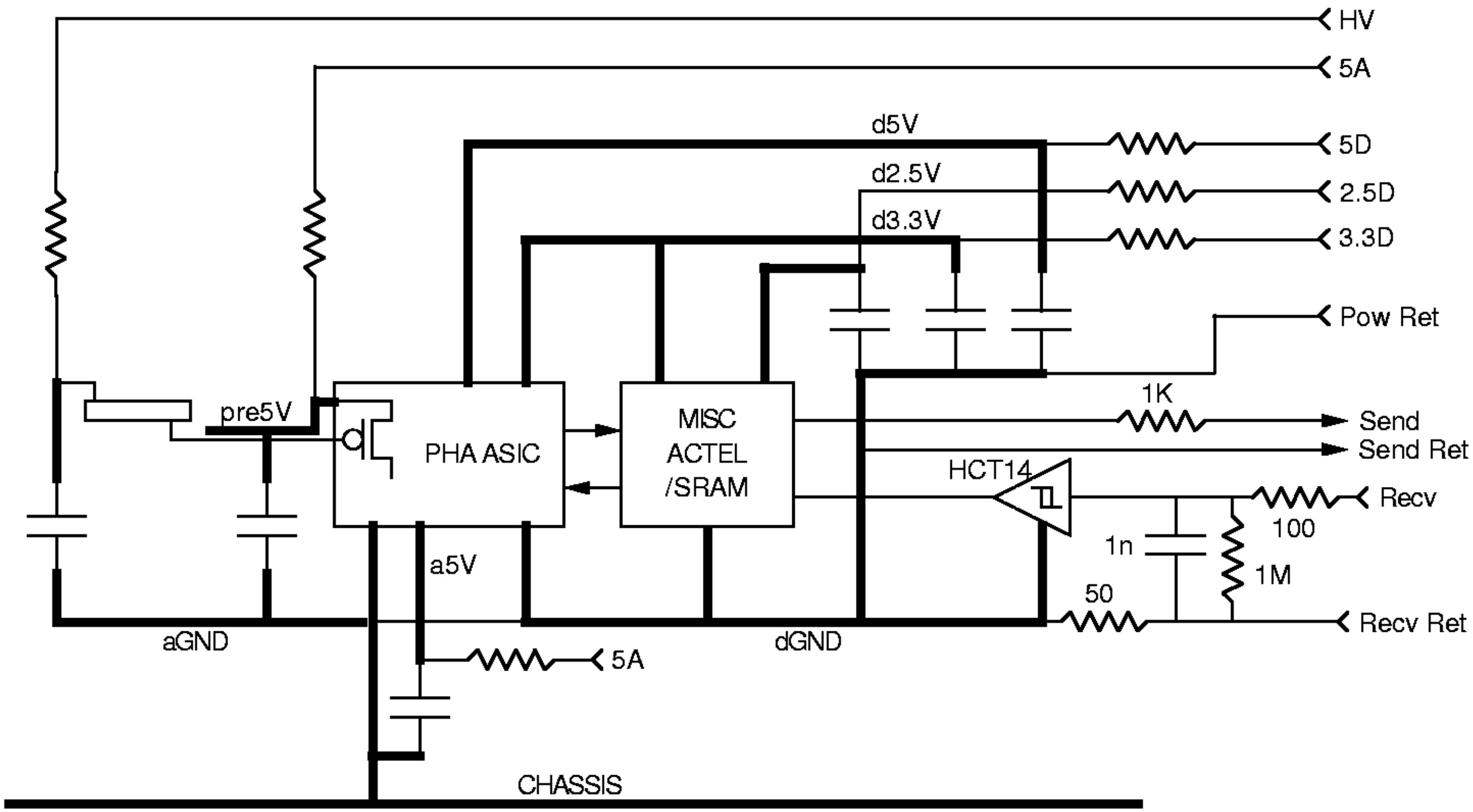
LET Electronics


Low Energy Telescope (LET)
FRAME SYNC
RESET
COMMAND
RESPONSE
DATA
SEP DPU
L1A
L2A
L3A
L3B
L2B
L1B
15
10
2
2
10
15
PHA ASIC
PHA ASIC
PHA ASIC
PHA ASIC
PHA ASIC
PHA ASIC
L1AOR
L2AOR
L3AOR
L3BOR
L2BOR
L1BOR
24
DATA
CONTROL
MISC ACTEL 54SX72
DATA
ADDRESS
CONTROL
SRAM 128K x 24
TEMP
+5A
+5D
+3.3D
+2.5D
DET.
BIAS
SEP DPU


MISC ACTEL for LET
FRAME SYNC
CMD IN
RCV UART
CMD OUT
SEND UART
DATA OUT
SEND UART
Int0-6
MISC
DATA INPUT
Gin0-23
ReadClk
Gout0-23
A0-17
D0-23
CONTROL
Output Register
Timers
L1AOR
L2AOR
L3AOR
L1BOR
L2BOR
L3BOR
Event Controller
CONTROL
Livetime Counter
ADCOR Counter


LET Event Controller Flow
Reset PHAs
Trigger ?
N
Inc. Livetime Counter
Y
Inc. Livetime Counter and ADCOR Counter
Wait 0.5 usec
Latch Tag Bits and Close Linear Gates
Wait for Rundowns
Valid Coinc. ?
N
Y
Interrupt MISC
Wait for PHA Readout

LET/HET Grounding/Interface



STEREO PHA ASIC

1) Complete front-end signal pulse processing for Silicon detectors in LET, HET and SIT.

2) Contains 16 complete dual-gain PHAs, each with:
   - A) Preamplifier, configurable to various detector capacitances and signal amplitude ranges.
   - B) Two complete shaping amplifier-linear gate-Wilkinson ADC chains, with combined dynamic range of 10000 (F.S./threshold).
   - C) Programmable thresholds
   - D) Bias switching to enable or disable power.
   - E) Scalar (23 bits) for counting trigger rate.

3) Pulse processing chain architecture due to H. Marshall, with 25 years of development/use in numerous space applications.

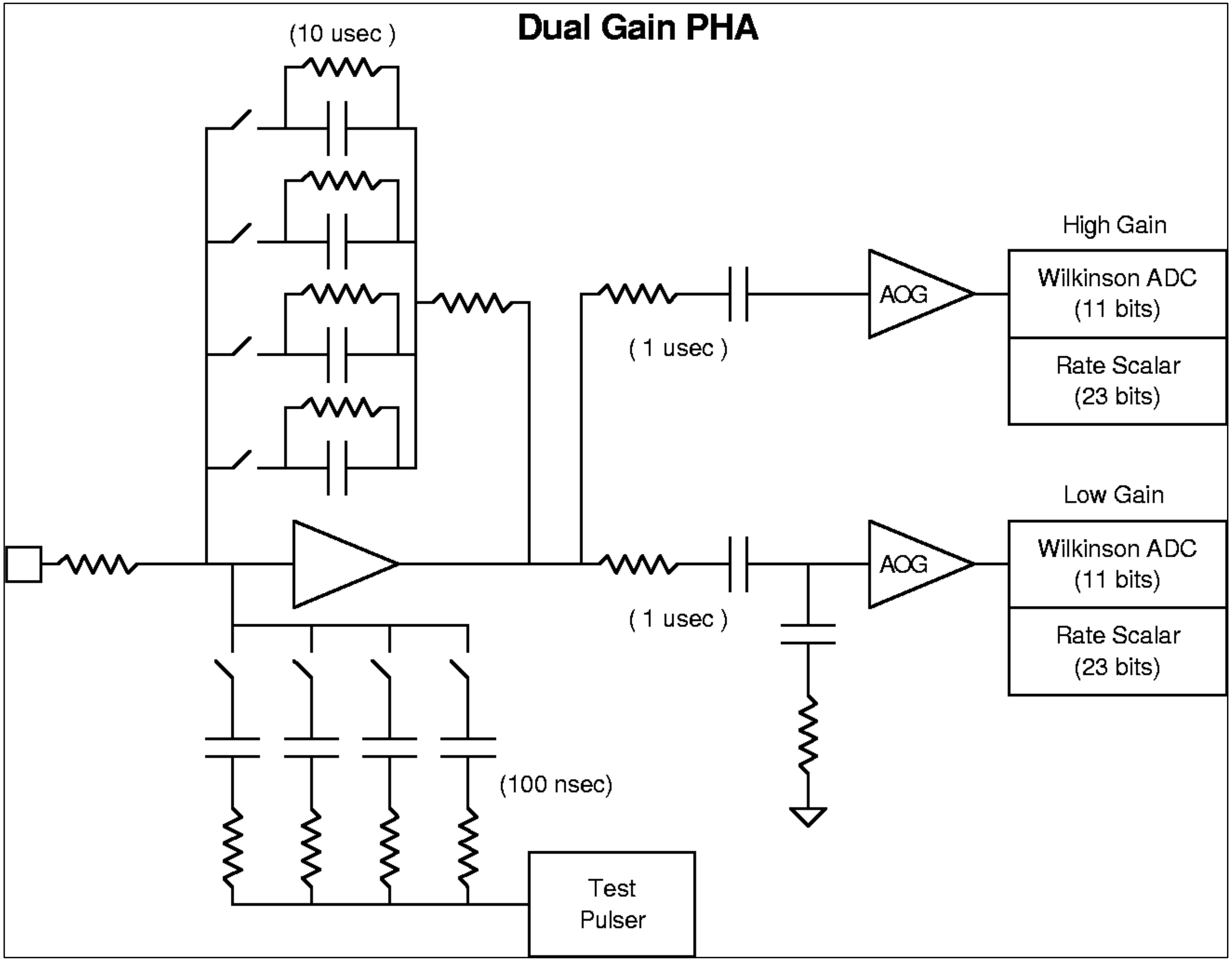
4) Evolution from ASIC developed for Advanced Composition Explorer:
   - A) Bipolar ---> CMOS
   - B) Critical passives off-chip ---> Most critical passives on-chip
   - C) No digital on-chip ---> Complete digital support on-chip
   - D) Dynamic range: 2000 ---> 10000
   - E) Max ADC conversion time 256 usec ---> 64 usec
   - F) Shaping time constants: 2 usec ---> 1 usec.
   - F) Power consumption (per chain) 40 mW ---> 9 mW.

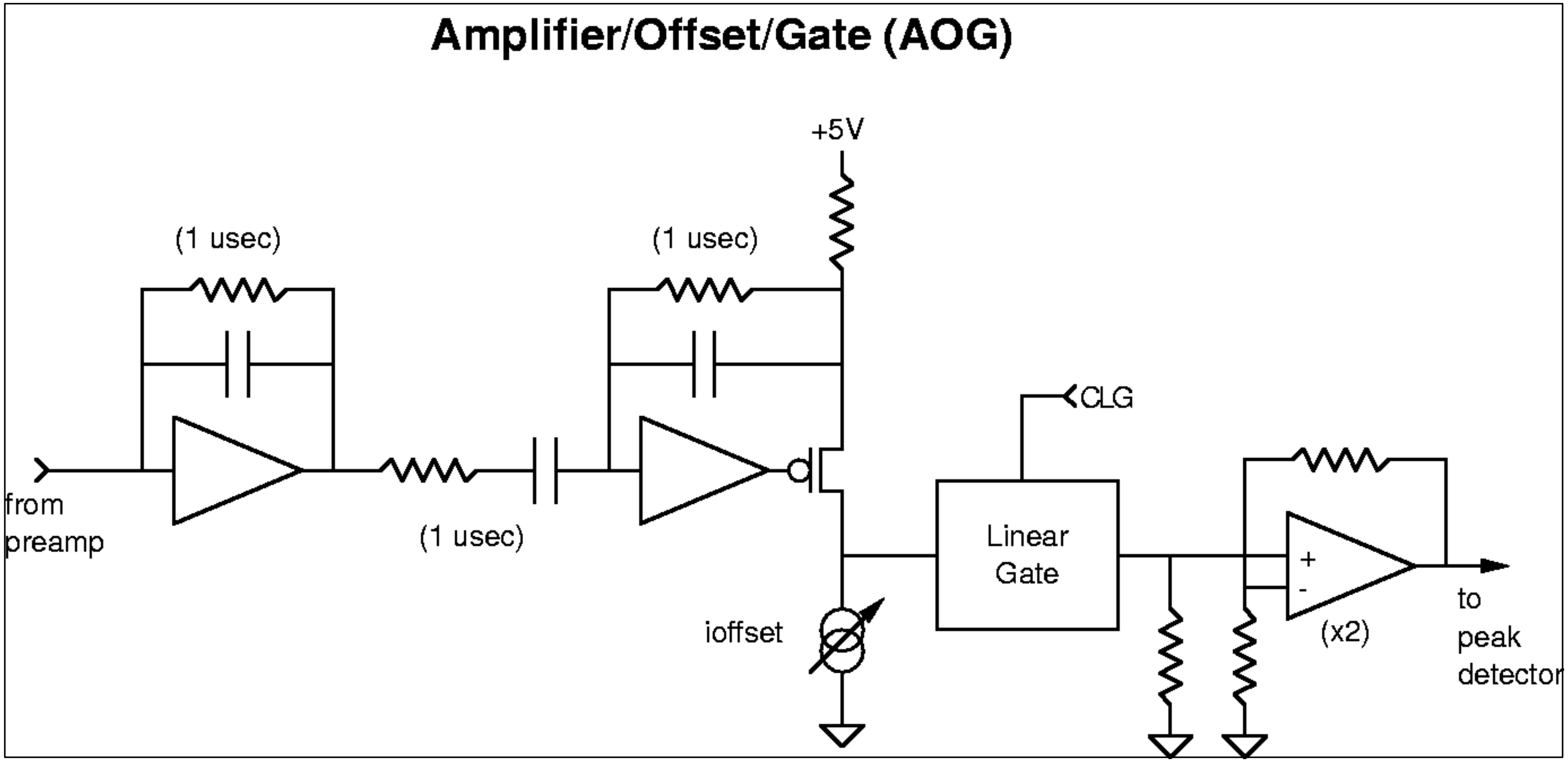
STEREO PHA ASIC Development

1) Experience with AMI 0.5 uM "C5N" fab gained through MOSIS:
   A) Prototype of critical pulse chain elements (2 runs)
   B) Prototype of pixel detector readout for gamma-ray telescope.
   C) First-time success on all analog functions ---> accurate SPICE modeling achieved.
   D) Noise performance verified, SPICE noise parameters measured.
   E) Process characterized down to 85K in collaboration with MOSIS.

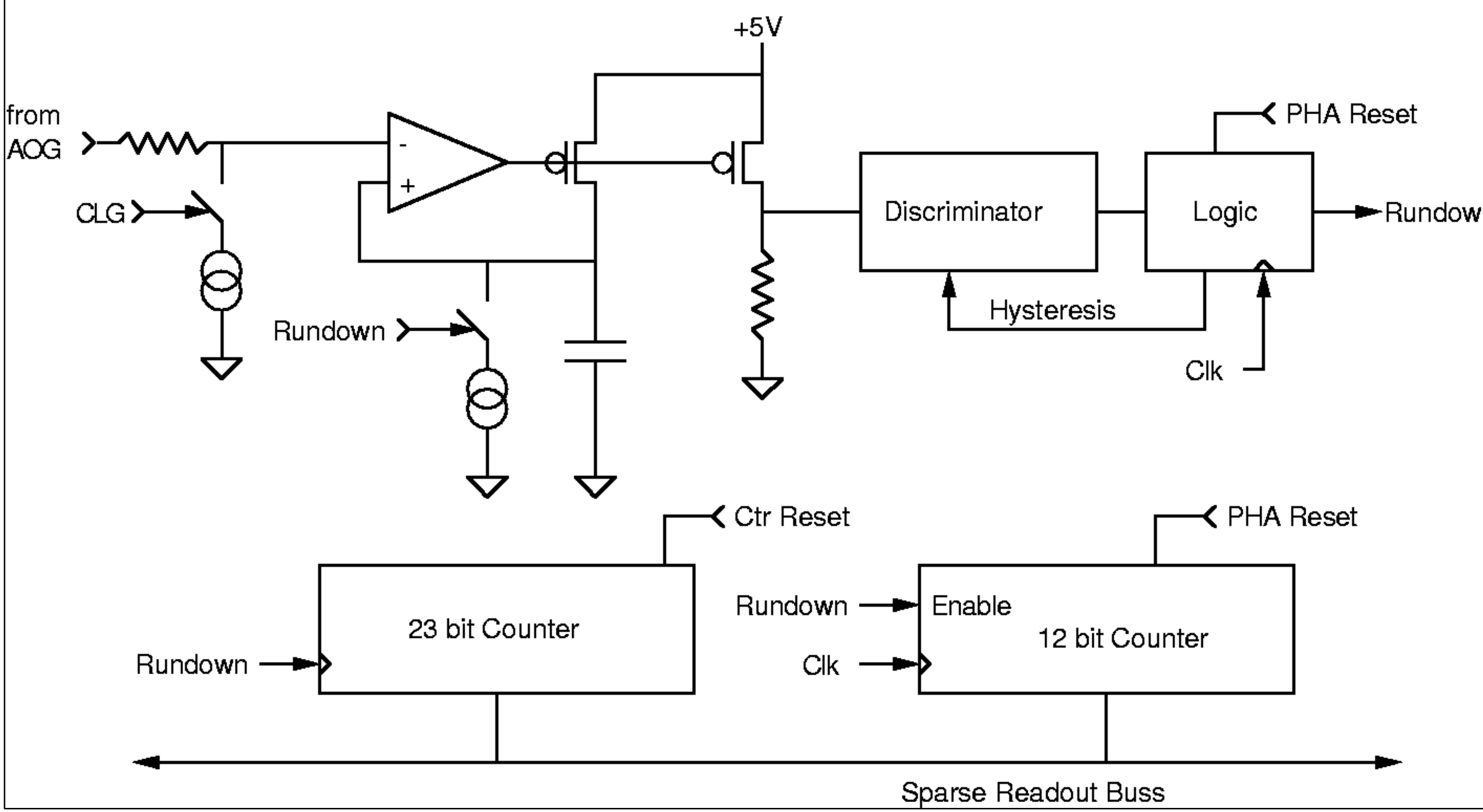
2) Key Development Milestones:
   A) PHA ASIC user's manual distributed to team members mid-May 2001.
   B) Chip schematics completed mid-Aug. 2001.
   C) Chip fab submission Oct. 2001
   D) Receive wafers Jan. 2001
   E) Prototype hybrids available Feb. 2001.

4) Rad-tolerance:
   A) "Hardness-by-Design" methodology should yield high latch-up threshold (via guard banding).
   B) Total dose tolerance should exceed requirements
   B) Plan latch-up threshold testing with help of Aerospace Corp. and total dose testing at JPL.
   C) Backup plan -- respin with UTMC rad-hardening process additions.


Dual Gain PHA
(10 usec)
(1 usec)
(1 usec)
High Gain
AOG
Wilkinson ADC
(11 bits)
Rate Scalar
(23 bits)
Low Gain
AOG
Wilkinson ADC
(11 bits)
Rate Scalar
(23 bits)
(100 nsec)
Test
Pulser

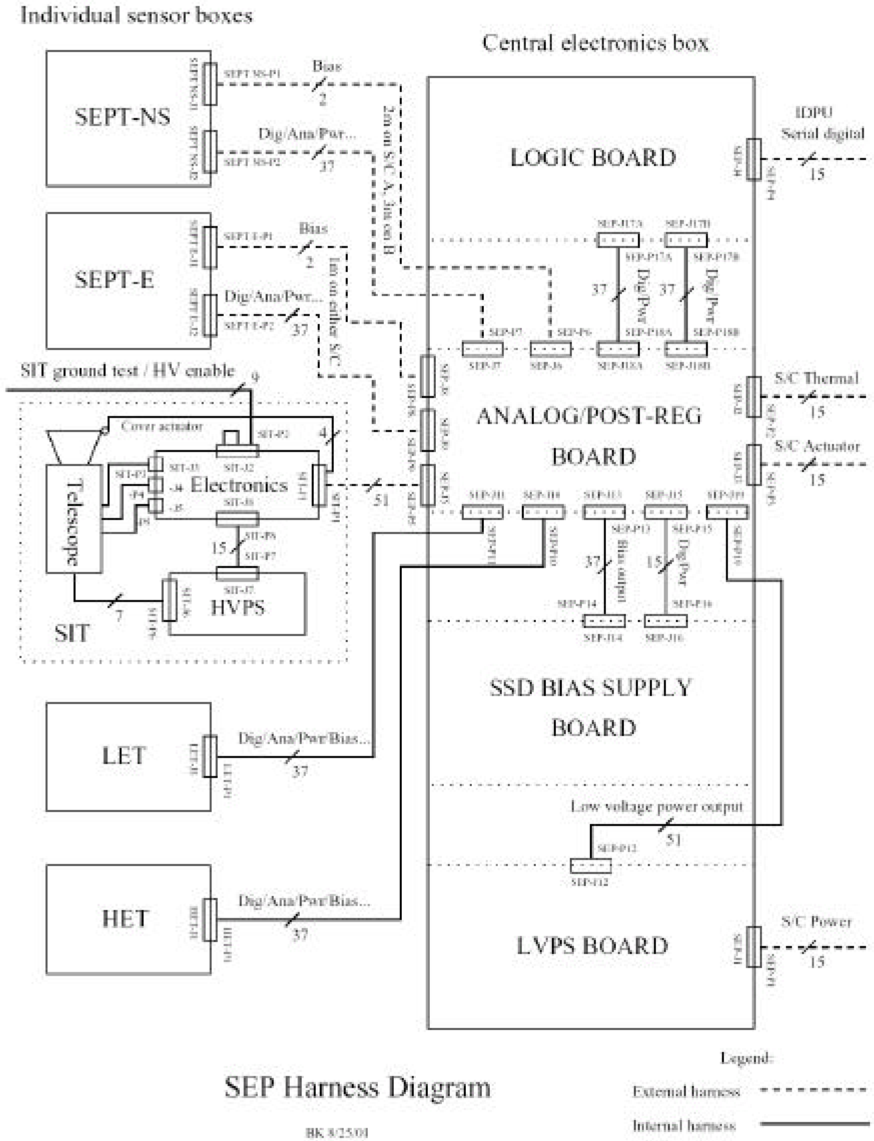

Amplifier/Offset/Gate (AOG)
+5V
(1 usec)
(1 usec)
CLG
from
preamp
(1 usec)
Linear
Gate
+
-
to
peak
detector
ioffset
(x2)

Wilkinson ADC and Rate Scalar



SEP Central Electronics

STEREO SEP Block Diagram



Low Voltage Power Supply

- Design and fab by UC Berkeley.
- Voltage & load requirements ~90% defined.
- Outputs include:
  - +2.5V, +3.3V, +5V, -5.2V (all digital, used directly)
  - +13V, -13V (used in SIT and SSD bias supplies)
  - +5.5V (used to generate analog +5V)
- May need -5V for HK ADC but will try to find lower power ADC that doesn't require it.
- Connector type and size selected. Pin assignments not yet defined.

SEP LVPS Voltage Requirements 9/11/01

Voltage	Type	SEPT	SIT	LET	HET	Central	LVPS out
2.5 V	Digital	X	X	X	X	X	**2.5 V**
3.3 V	Digital		X	X	X	X	**3.3 V**
5.0 V	Digital	X	X	X	X	X	**5.0 V**
-5.2 V	Digital		X			X	**-5.2 V**
13.0 V	Analog		X			X	**13.0 V**
-13.0 V	Analog		X			X	**-13.0 V**
5.0 V	Analog	X	X	X	X	X	**5.5 V**

SEP LVPS Load Requirements [mW] 9/11/01

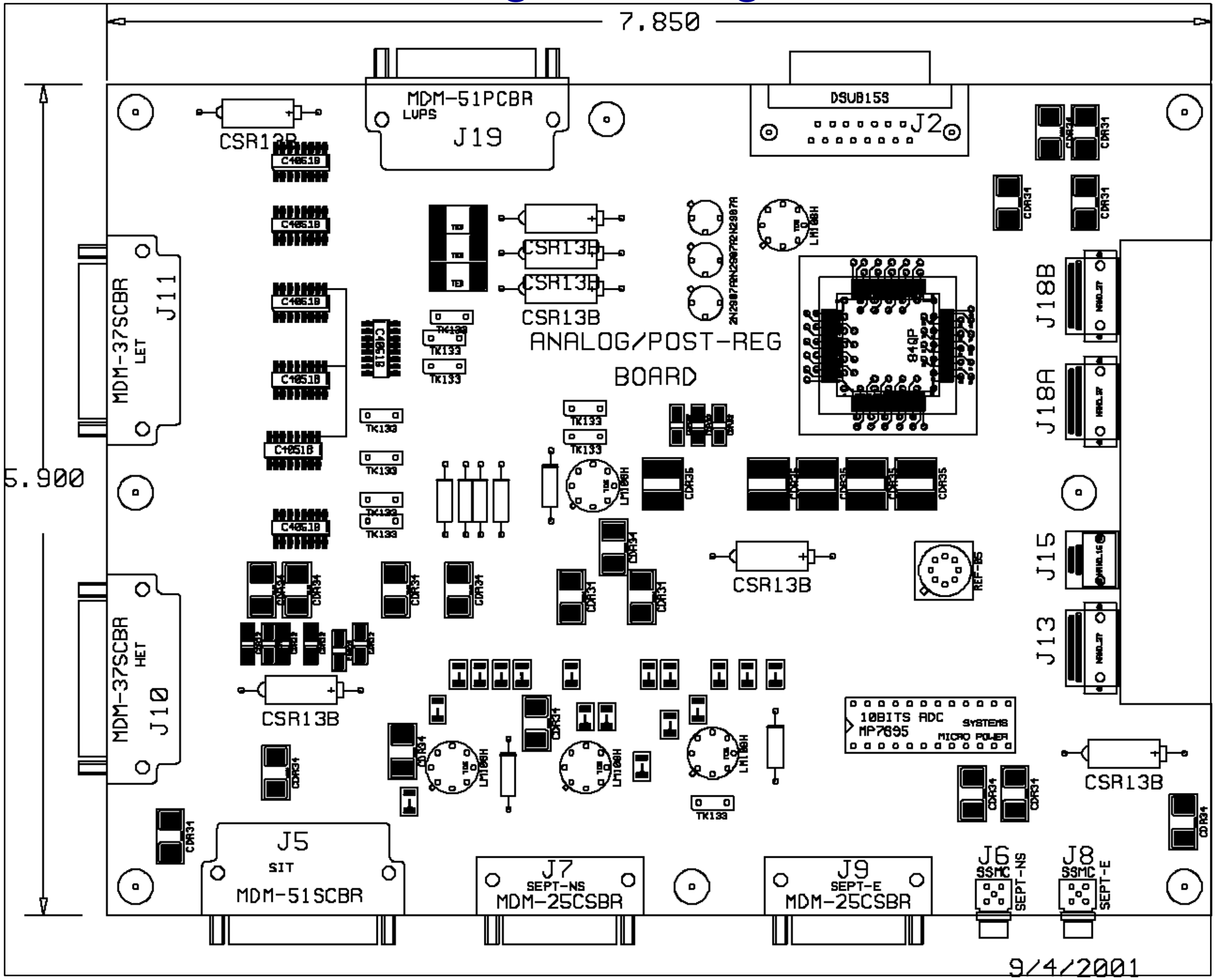
Voltage	Type	SEPT	SIT	LET	HET	Central	Totals
2.5 V	Digital	50	25	43	43	25	**185**
3.3 V	Digital		227	181	181	95	**684**
5.0 V	Digital	345	56				**401**
-5.2 V	Digital	5*	464	25*	25*	25*	**544**
13.0 V	Analog		196			171	**368**
-13.0 V	Analog		57			151	**208**
5.5 V	Analog	605	248	526	103	62	**1544**
		------	------	-----	-----	-----	------
Instr. Subtotals:		**1005**	**1273**	**774**	**352**	**529**	**3933**
LVPS consumption @ 65% efficiency:							**2118**
SEP total consumption:							**6051**

* Regulated voltage used (–5V instead of –5.2V).

Analog/Post-Reg Board

- Functions:
  - Regulation/distribution of low voltage power
  - Routing of interface signals
  - Housekeeping ADC
- Design and fab by Space Instruments, Inc., with close Caltech supervision.
- Electrical definition ~80% complete:
  - Number and type of connectors known.
  - Outside I/F connector pin assignments defined.
  - Regulator input/output voltages and loads defined.
  - List of HK items preliminary (voltages, temps, etc.).
- Preliminary mechanical interface is defined, with connector locations specified.

Analog/Post-Reg Board



SSD Bias Supply Requirements

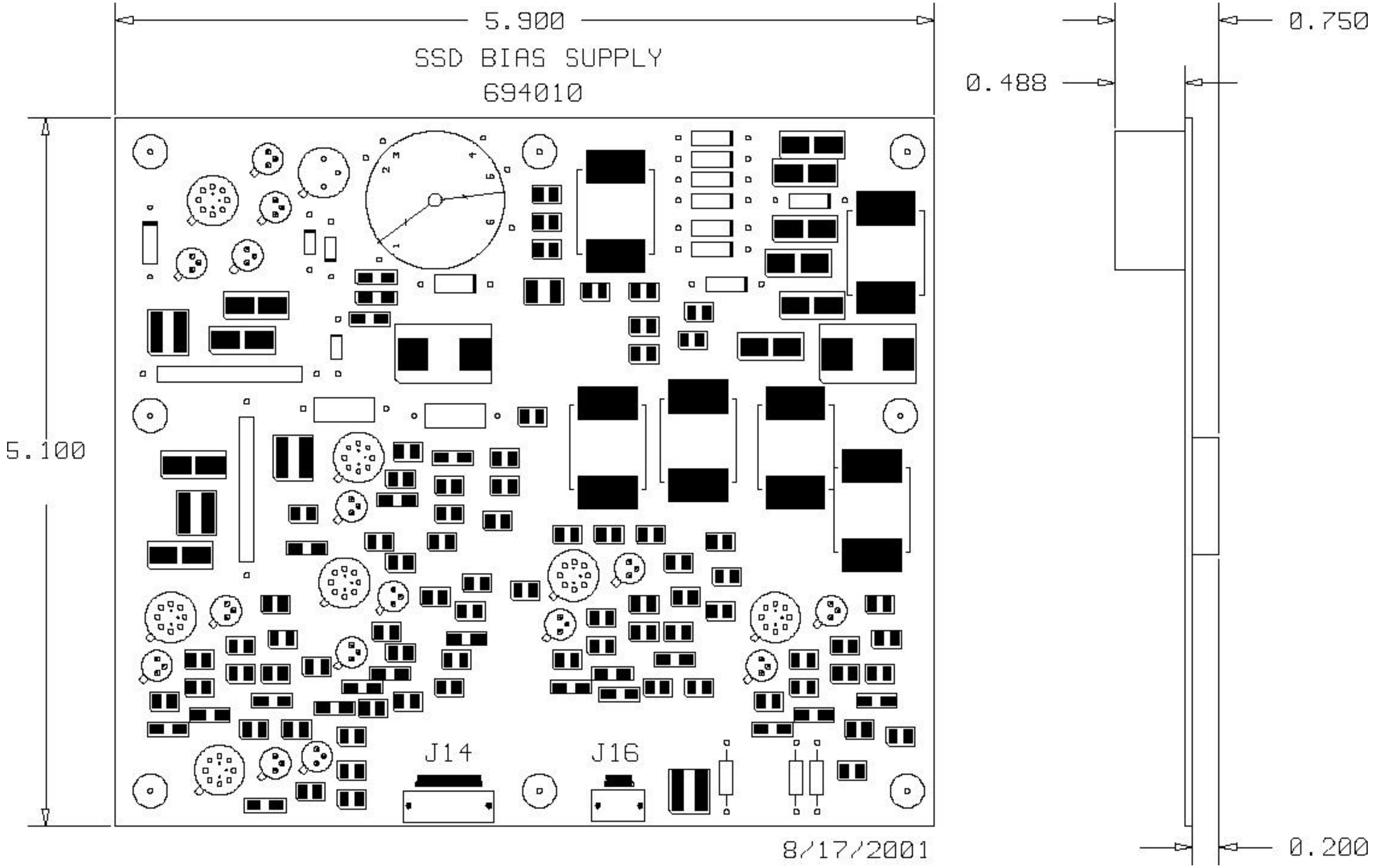
Bias Signals	Nominal Voltage	Voltage Range	Max. Current
LET L1	10V	2 - 30V	150uA
LET L2	30V	5 - 50V	20uA
LET L3 &	250V	50 - 250V	60uA
HET H1-6	“	“	130uA
SIT SSD	160V	150 - 200V	15uA
SEPT	-80V	-30 - -80V	65uA

(Ripple < 0.2mVpp; Spikes < 1mVpp)

(Input +/-13V; Power dissipation ~200mW + output power)

• Design and fab by Space Instruments, Inc.

SEP Bias Supply



Logic Board (SEP DPU)

Contains:

- **MISC processor with 128k x 24 SRAM and 128k x 24 EEPROM**
- **Digital interfaces with SIT, HET, LET, SEPT and IMPACT IDPU (defined by ICDs)**
- **Interface with HK ADC (ADC to be selected yet.)**
- **On/off control of SSD Bias Supplies**
- **Operational heater control**
- **Mechanical interface TBD, approx. size: 15 x 20 cm**

Parts

- Logic:
  - RT54SX72S - Actel FPGA
  - HLX6228 - Honeywell SRAM, 128k x 8
  - 28LV010RP - Space Electronics with Hitachi EEPROM, 128k x 8
  - HCTS14MS – generic interface buffer
  - HCS244KMSR – generic interface buffer
  - Q-TECH 16 and 32 MHz clock oscillators
- Discrete:
  - will use grade 2 or better. Spare ACE parts available, pending evaluation and recommendation of JPL or project.
- Custom VLSI:
  - PHA ASIC chip to be fabbed at AMIS, used in hybrid fabbed at JPL. VLSI chip screening spec to be developed with JPL help, following ACE chip model.

Connectors

- **Originally planned low-mass Nanonics connectors for both internal and external interfaces.**
- **Now plan to use Nanonics only for internal cables, use MDM for external, as result of Peer Review recommendations.**
- **Plan redundant wires in all cables – issue of mass for SEPT cables, which have moved far away from central electronics box.**
- **Issue of coax for SEPT bias: will be reviewing the need for coax and SEPT HV filtering design.**

SEP resources: Mass [g] 9/11/01

Component	PDR	Peer Rev.	
SIT sensor & door	500	500	
SIT elec. boards & wiring	370	370	
SIT HVPS	160	160	
SIT encl. & hdwr	200	200	
SIT subtotal:	**1230**	**1230**	
SEPT-NS	520	520	w/o harness
SEPT-E	520	540	w/ 10cm harness
SEPT subtotal:	**1040**	**1060**	
LET det. & housing	515	515	
LET electronics	235	235	
LET subtotal:	**750**	**750**	
HET det. & housing	500	460	
HET electronics	160	160	
HET subtotal:	**660**	**620**	
Cent. elec. encl. & hdwr	1500	1030	
El. boards, shields, harness	1090	1090	
Central electr. subtotal:	**2590**	**2120**	
SEPT-NS bracket	270	270	
LET bracket	600	600	
SEP bracket	N/A	N/A	
SEP total:	**7140**	**6650**	

SEP resources: Mass [g] 9/11/01

Component	PDR	Peer Rev.
SEPT-NS Ahead harness (1.7 m)	185	150
SEPT-NS Behind harness (2.9 m)	293	150
SEPT-E Ahead harness (0.4 m)	73	N/A
SEPT-E Behind harness (2.3 m)	240	N/A
Thermal blankets	120	100
SEP Ahead total:	**7518**	**6900**
SEP Behind total:	**7793**	**6900**

Note: The increased harness weights are to be covered by the Project as part of the solution to SEP field-of-view problems associated with the new spacecraft configuration. This still leaves an overall weight growth of 510 g (7.4%)

SEP resources: Power [mW] 9/11/01

Component	PDR	Peer Rev.
SIT HVPS & energy el.	473	575
TOF CFD (from STEP)	680	610
MISC @ 4 MHz	120	190
SIT subtotal:	**1273**	**1375**
SEPT	**1005**	**1000**
LET VLSI	486	250
HK ADC	65	N/A
MISC @ 8 MHz	223	185
LET subtotal:	**774**	**435**
HET VLSI	63	65
HK ADC	65	N/A
MISC @ 8 MHz	223	185
HET subtotal:	**351**	**250**
Analog/Post-reg	210	240
Logic (MISC @ 4MHz)	120	150
SSD bias supply	200 @ +20 C *	180
Central electr. sub.:	**530**	**570**
LVPS (65% eff.)	2118	1955
SEP total:	**6051**	**5585**

* SSD bias supply capable of consuming 313 mW @ +35 C & end of detector life.

SEP resources: Data rate [bit/s] 9/11/01

Component	**PDR**	**Peer Rev.**
SIT	240	240
SEPT	60	60
LET	320	320
HET	120	120
Central electronics	0	0
------------------------	------	------
SEP total:	**740**	**740**

SEP Flight Software

STEREO SEP Flight Software

Personnel and Responsibilities

- **Caltech – LET, SEPT and SEP DPU**
  - **Rick Cook, Andrew Davis, Allan Labrador**

- **GSFC – HET and SIT**
  - **Don Reames, Tycho von Rosenvinge, Kristen Wortman, Bob Baker, Tom Nolan**

Flight Software Heritage/Experience

- **Caltech – SIS and CRIS instruments on ACE, and balloon instruments**
- **GSFC – EPACT instrument suite on WIND**

Applicable Documents

- STEREO IMPACT Performance Specification
- LET Science Requirements Document
- IMPACT SEP Flight Software Development Plan
  - Includes SEP Flight Software Requirements
- IMPACT/Spacecraft ICD
- IMPACT Intra-Instrument Serial Interface ICD
- SEP Instrument Suite ICD (in prep)
- P24 MISC G-buss I/O Interface Doc (in prep)
- P24 MISC Processor Manual
- LET Science Data Frame Format Specification
- Flight Software Users Manual

Top-Level Requirements

- **Collect science data from HET, LET, SEPT, SIT**
- **Collect housekeeping data from SEP instruments and other SEP subsystems (power supplies, bias supplies, etc)**
- **Manage setup and mode control of SEP instruments and other SEP subsystems**
- **Interface with IMPACT IDPU**
  - **Process commands received through IDPU interface**
  - **Format SEP science and housekeeping data and send to IDPU**

(See SEP block diagram)

Top-Level Requirements (2)

Caltech will develop three software packages:

- **SEP Common Software:** Forth operating system, common interface routines, utility functions common to all MISCs
- **SEP Software:** software routines unique to SEP MISC
- **LET Software:** software routines unique to LET

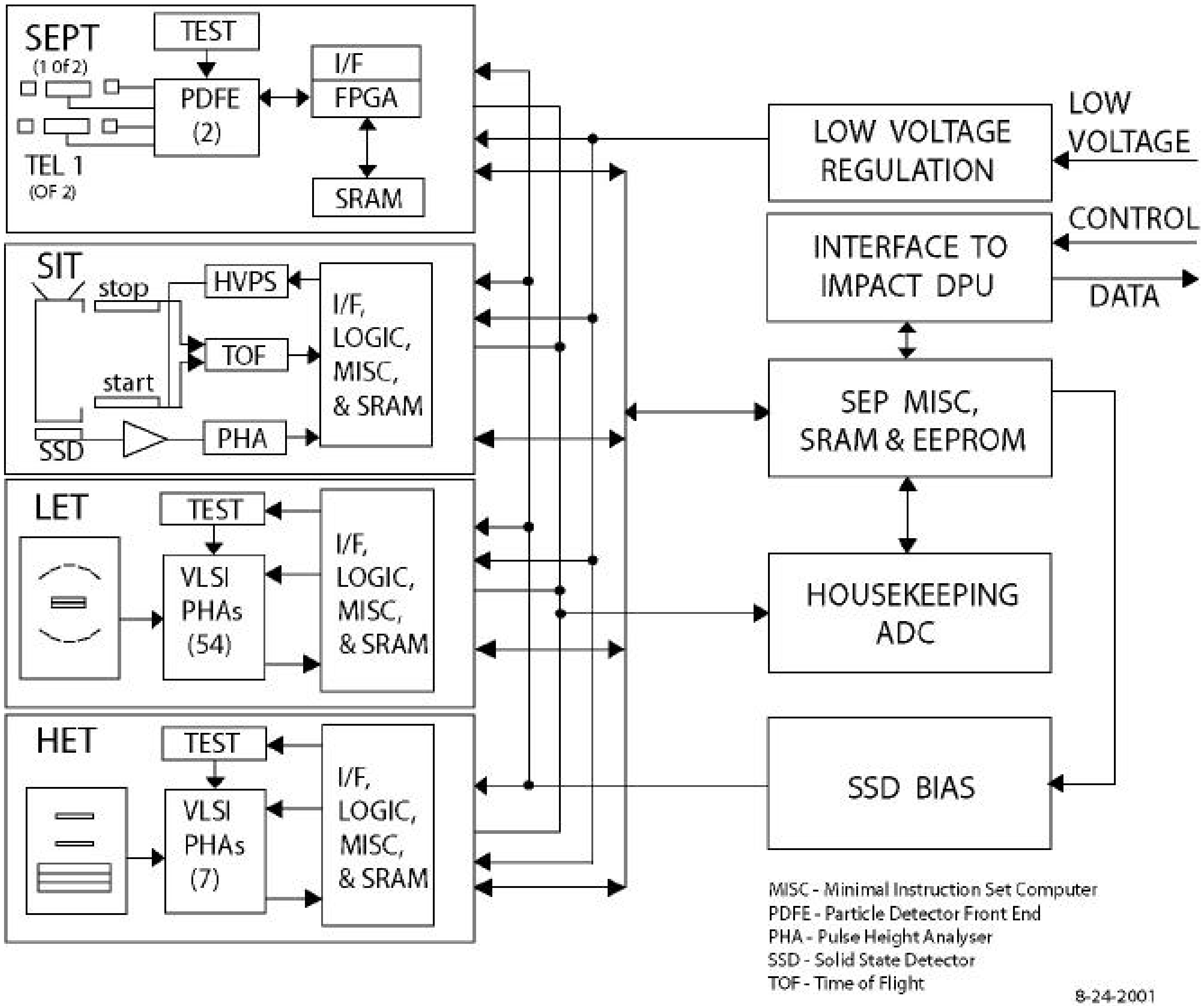
GSFC will develop two software packages:

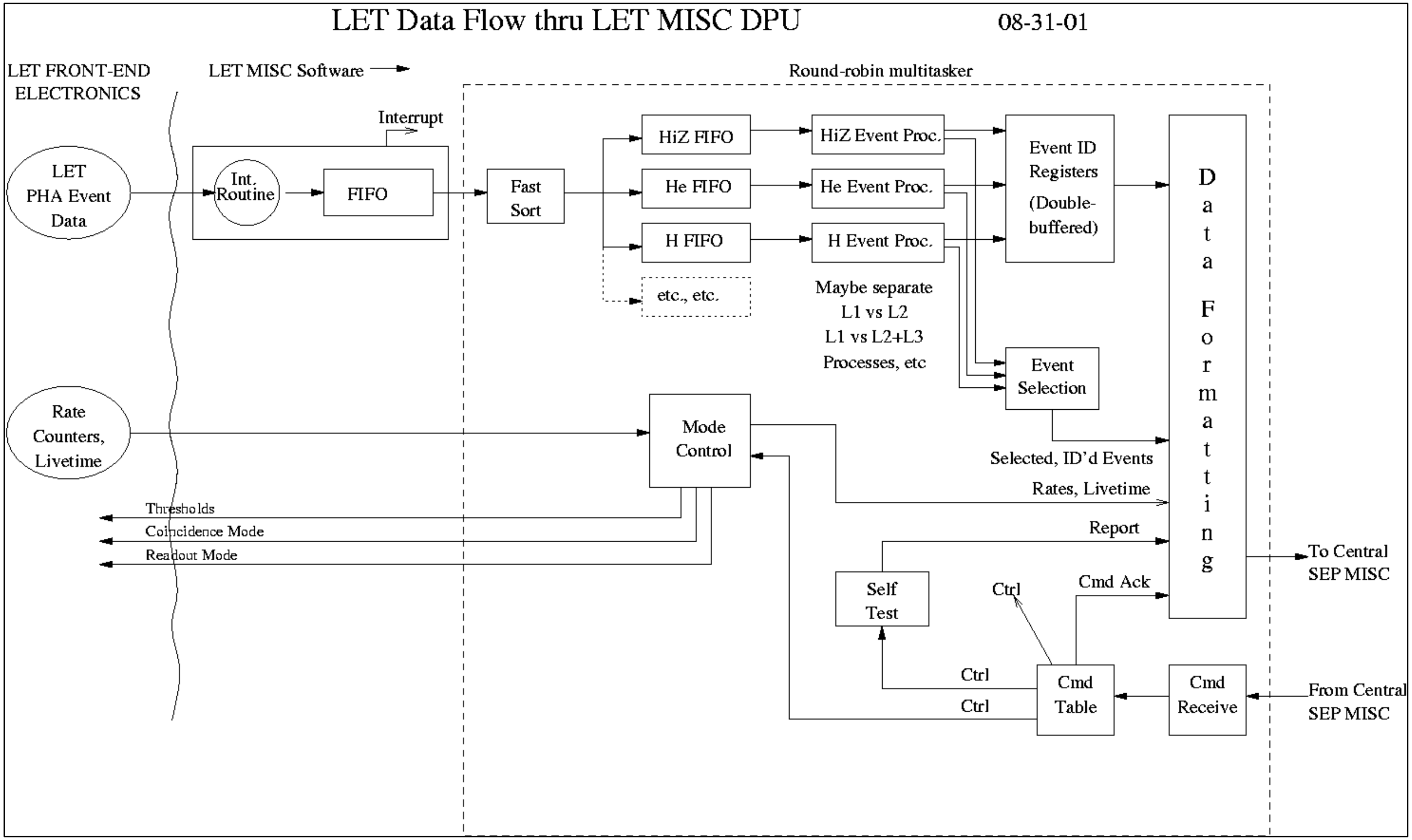
- **HET Software:** software routines unique to HET
- **SIT Software:** software routines unique to SIT

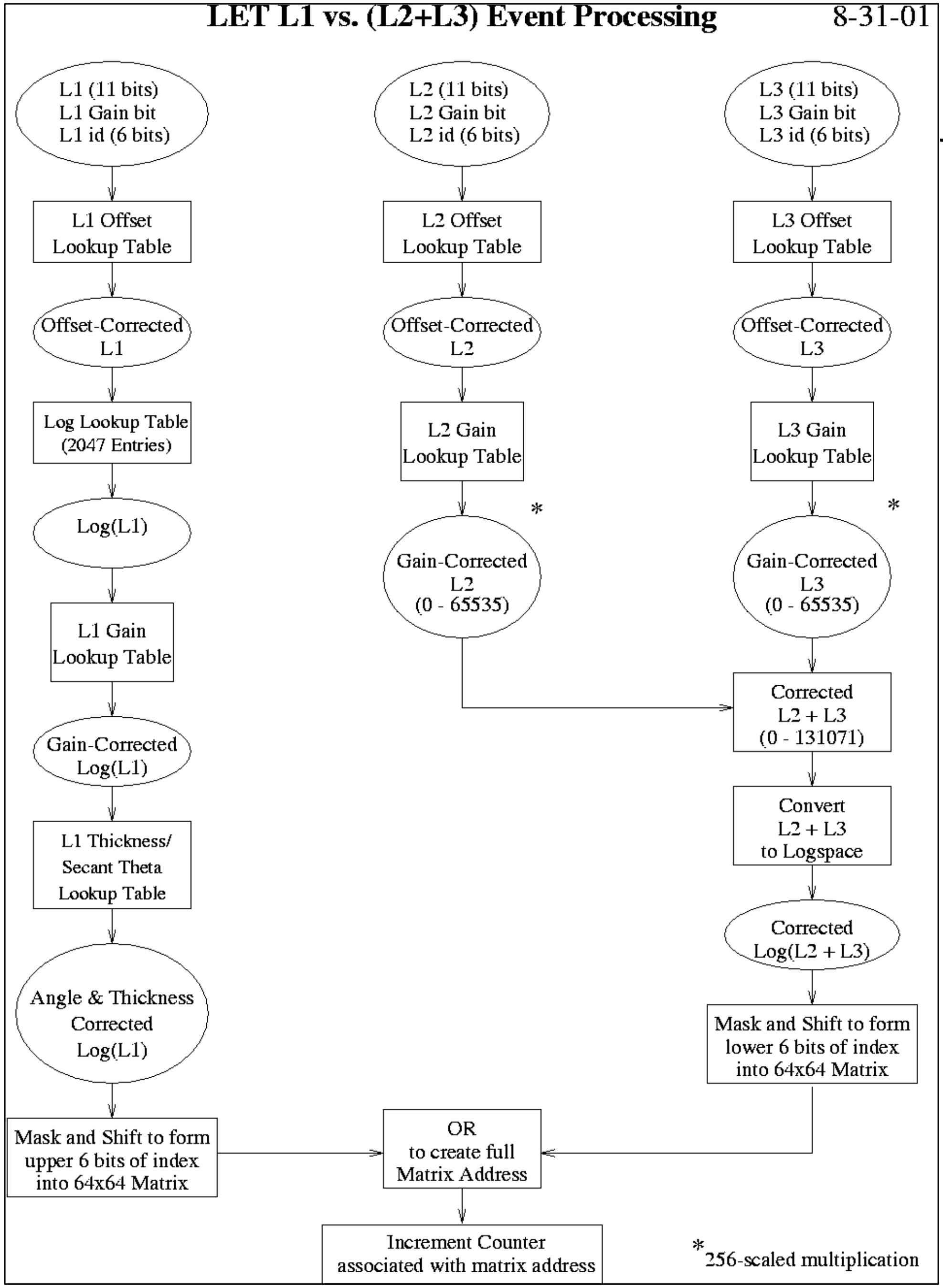
Detailed Requirements

The Software Requirements below are defined in the SEP Software Development Plan (SDP).

- Memory, CPU performance
- Operating System
- Power-on Initialization
- Interfaces and common utility functions
- Science Data Acquisition
- Science Data Processing
- Beacon Data
- Housekeeping and Status Data Acquisition
- Data Formatting
- Command Processing
- Functional Tests
- Reliability


SEPT
(1 0f 2)
TEST
PDFE
(2)
I/F
FPGA
SRAM
TEL 1
(OF 2)
SIT
stop
start
SSD
HVPS
TOF
PHA
I/F,
LOGIC,
MISC,
& SRAM
LET
TEST
VLSI
PHAs
(54)
I/F,
LOGIC,
MISC,
& SRAM
HET
TEST
VLSI
PHAs
(7)
I/F,
LOGIC,
MISC,
& SRAM
LOW VOLTAGE
REGULATION
LOW
VOLTAGE
INTERFACE TO
IMPACT DPU
CONTROL
DATA
SEP MISC,
SRAM & EEPROM
HOUSEKEEPING
ADC
SSD BIAS
MISC - Minimal Instruction Set Computer
PDFE - Particle Detector Front End
PHA - Pulse Height Analyser
SSD - Solid State Detector
TOF - Time of Flight
8-24-2001


LET Data Flow thru LET MISC DPU
08-31-01
LET FRONT-END ELECTRONICS
LET MISC Software
Round-robin multitasker
Interrupt
LET PHA Event Data
Int. Routine
FIFO
Fast Sort
HiZ FIFO
He FIFO
H FIFO
etc., etc.
HiZ Event Proc.
He Event Proc.
H Event Proc.
Event ID Registers (Double-buffered)
Maybe separate L1 vs L2 L1 vs L2+L3 Processes, etc
Event Selection
Data Formatting
Selected, ID'd Events
Rates, Livetime
Report
Cmd Ack
To Central SEP MISC
From Central SEP MISC
Rate Counters, Livetime
Mode Control
Thresholds
Coincidence Mode
Readout Mode
Self Test
Ctrl
Ctrl
Ctrl
Cmd Table
Cmd Receive


LET L1 vs. (L2+L3) Event Processing
8-31-01
L1 (11 bits)
L1 Gain bit
L1 id (6 bits)
L2 (11 bits)
L2 Gain bit
L2 id (6 bits)
L3 (11 bits)
L3 Gain bit
L3 id (6 bits)
L1 Offset Lookup Table
L2 Offset Lookup Table
L3 Offset Lookup Table
Offset-Corrected L1
Offset-Corrected L2
Offset-Corrected L3
Log Lookup Table (2047 Entries)
L2 Gain Lookup Table
L3 Gain Lookup Table
Log(L1)
*
Gain-Corrected L2 (0 - 65535)
*
Gain-Corrected L3 (0 - 65535)
L1 Gain Lookup Table
Corrected L2 + L3 (0 - 131071)
Gain-Corrected Log(L1)
Convert L2 + L3 to Logspace
L1 Thickness/ Secant Theta Lookup Table
Corrected Log(L2 + L3)
Angle & Thickness Corrected Log(L1)
Mask and Shift to form lower 6 bits of index into 64x64 Matrix
Mask and Shift to form upper 6 bits of index into 64x64 Matrix
OR to create full Matrix Address
Increment Counter associated with matrix address
*256-scaled multiplication

Rick Cook

Software Design Methodology

Top-Down and Bottom-Up Approaches running in parallel

- **Top-Down**
  1. **Requirements definition and analysis**
  2. **Design Phase**
  3. **Implementation**
  4. **System testing and acceptance testing**
- **Bottom-Up**
  1. **Develop small test routines – gain familiarity with MISC processor**
  2. **Verify Forth system on MISC with standard software test suite**
  3. **Prototype onboard processing algorithms to verify feasibility of MISC hardware approach**

Top-Down Software Development Phases

1. Requirements definition and analysis
   – Starting with the SEP science requirements, the software requirements listed earlier will be defined and documented in the SDP
2. Design Phase
   – Define system architecture, sort requirements into subsystems, define internal and external interfaces. Produce a set of design specifications
3. Implementation
   – Build flight software from design specs. Forth and assembly language. Use coding guidelines and standards defined in SDP
4. System testing and acceptance testing
   – Accelerator test, radiation sources, built-in self-test routines, test procedures
   – Software walkthroughs, regular reports

Development Environment

- Most software development and testing done on engineering test units or flight units using resident Forth operating system
- Code - a mixture of modular, structured Forth and assembly language
- Serial communication link between development PC and MISC allows software uploads and direct interaction with resident Forth system
- Full simulation of MISC Forth system is available under Win32Forth
- Assembler for MISC is available under Win32Forth
- Expect a large number of intermediate software builds, tied to the development of the flight hardware

Software Quality Assurance Measures

- Only the lead engineer is authorized to load flight software into flight MISCs
- Lead engineer maintains flight source code. Developers deliver software modules to lead engineer for incorporation into the flight code
- Checksums calculated during EEPROM burn-in, checked during boot process
- Version numbering and documentation of changes for all source files
- Archiving and backup of all source code each day the code is worked on
- Formal version control and problem tracking during latter stages of implementation phase, prior to installation into flight hardware.
- Software walkthroughs at software peer reviews, reports at PDR and CDR
- System and acceptance tests : end-to-end instrument, electronics, and software functional tests done using accelerator tests, radiation sources, built-in self-test routines and test procedures
- More details in Software Development Plan

Current Status

- **Requirements Definition & Analysis**
  - Currently gathering instrument science data processing, housekeeping data and beacon data requirements from instrument teams
  - Data format definition is in progress – see LET Science Data Frame Format Document
  - Draft ICD between SEP DPU and IMPACT IDPU is written
  - SEP instrument suite ICD is in preparation
- **Preliminary Design**
  - Work begun on design/data flow diagrams (see LET data flow diagram)
  - Work begun on event processing algorithms for LET, HET and SIT

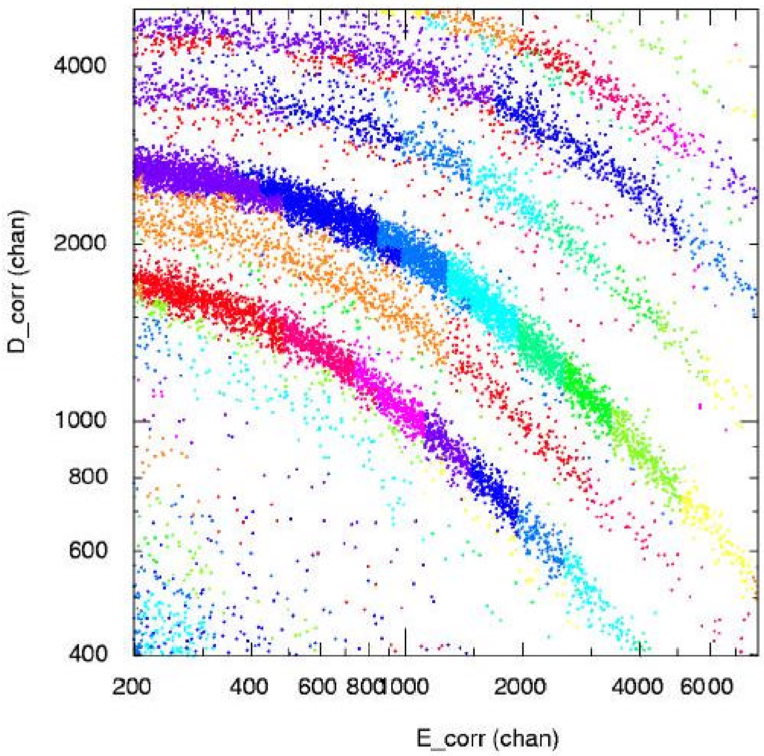
Current Status (2)

- **Prototyping**
  - Event processing algorithm for LET is implemented on the MISC in Forth
  - Same Forth code runs on the Harris RTX 2010, allowing for speed comparisons, and optimization of the MISC Forth system
  - Current version processes 13700 events/sec on MISC running at 10MHz

(see LET event processing algorithm flow diagram
and L1 vs. L2 matrix illustration)

- **MISC Forth System Functional Tests**
  - In progress, using a suite of standard Forth test routines

Illustration of Onboard Binning



A sample of pulse-height space from Wind/LEMT shows SW bins assigned in the onboard processing as different colors

Schedule Milestones

Item	Finish Date
Initial SEP Common Software	October 2001
SEP Common Software User Manual	October 2001
Final SEP Common Software	August 2002
Flight Software (LET, HET, SIT, SEP)	June 2003
Flight Software Testing	October 2003
Final User Manuals	October 2003

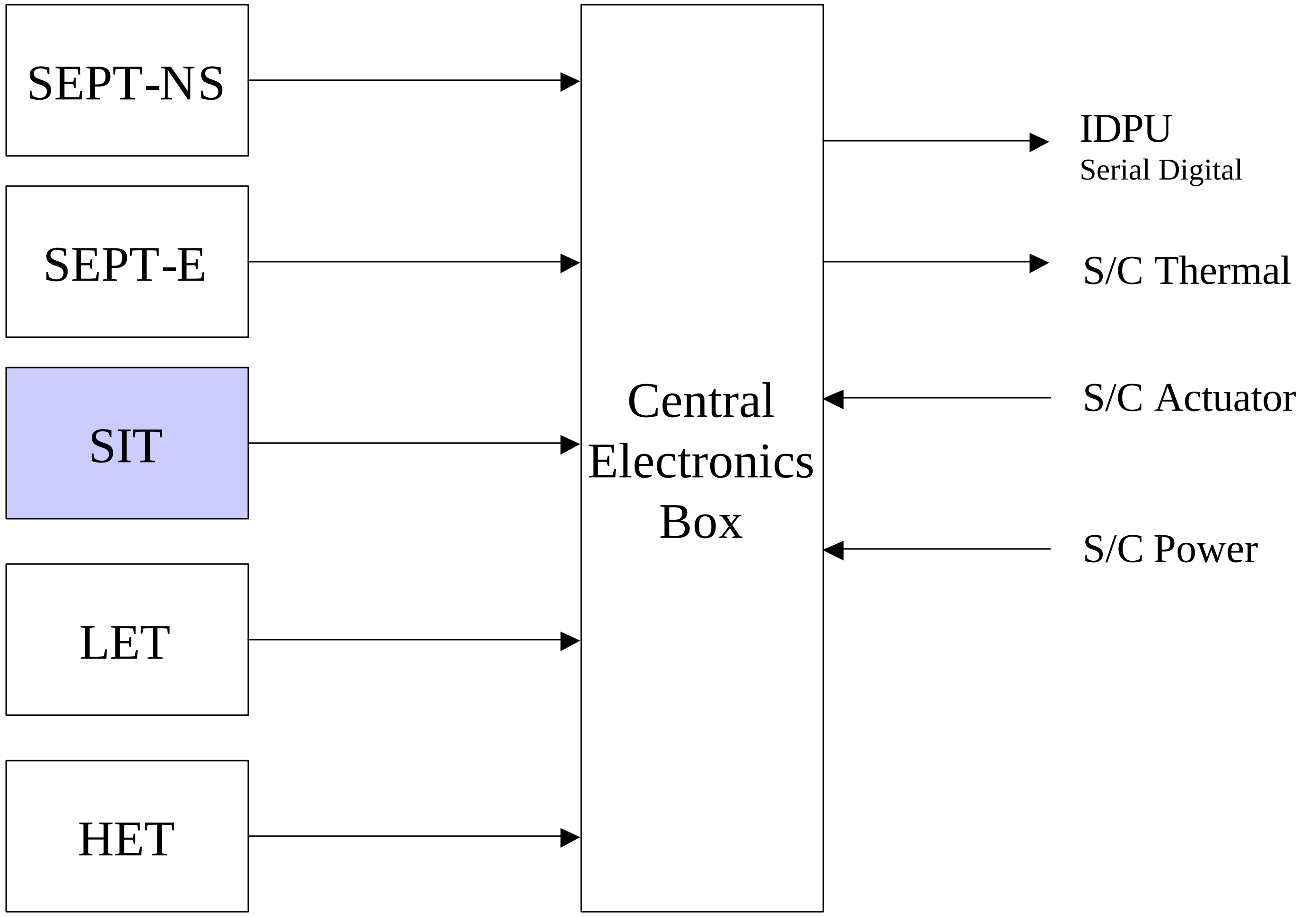
STEREO *IMPACT* PDR

SUPRATHERMAL ION TELESCOPE (SIT)

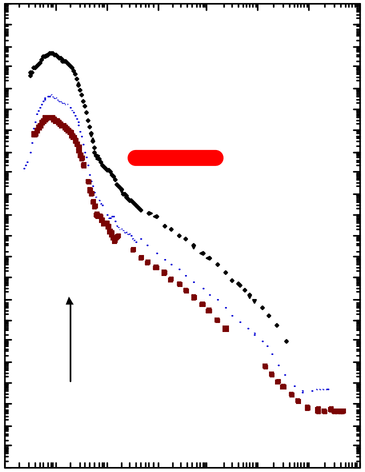
UMd
GSFC
MPAe
UCB

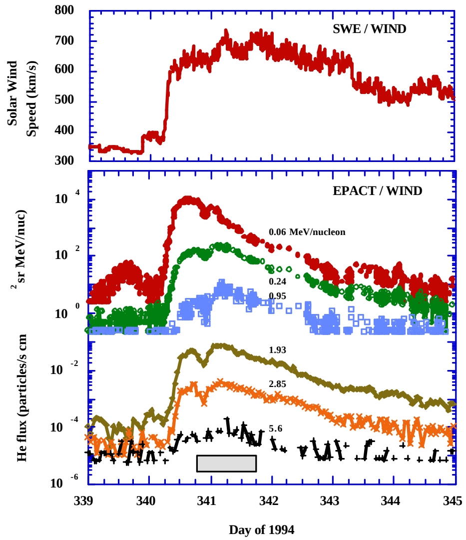
September 12, 2001

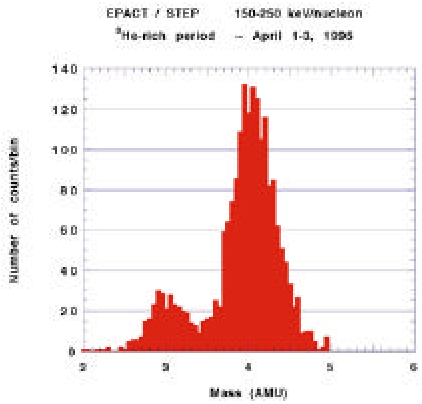
SEP Block Diagram



SIT -- Suprathermal Ion Telescope
Science & Performance Requirements







• *<u>energy range</u> -- range from solar wind to ~2 MeV/n*

•*<u>geometry factor</u> -- sufficient to measure heavy ion intensities*

• *<u>energy resolution</u> -- sufficient to construct spectra*

• *<u>FOV</u> -- observe large angle in ecliptic to intersect magnetic field as much as possible*

• *<u>max event rate</u> -- avoid saturation in intense events*

• *<u>time resolution</u> -- allow measurements of structures in interplanetary shocks, and as magnetic field wanders*

• *<u>mass resolution</u> -- sufficient to separate 3He vs 4He*

• *<u>background</u> -- low enough to resolve rare species*

figures (left to right) from Mewaldt, Mason, Gloeckler et al. 2001; Mason et al. 1997; Mason et al. 1995

SIT Performance Requirements

Description	Goal	Requirement
FOV	17 x 44 degrees	17 x 44 degrees
Energy	30-2000 keV/nuc, He-Fe	30-2000 keV/nuc, He-Fe
Mass Resolution	0.85 AMU (^{16}O at 100keV/nuc)	0.85 AMU (^{4}He at 1MeV/nuc)
Energy Resolution	20 keV FWHM	35keV FWHM @22C
Geometric Factor	0.4cm^2 ster	0.4cm^2 ster
Background	10^{-2} events/sec in quiet time	10^{-2} events/sec during vac test
Max Event rate	1000 events/sec	1000 events/sec
Time Resolution	1 minute	15 minutes

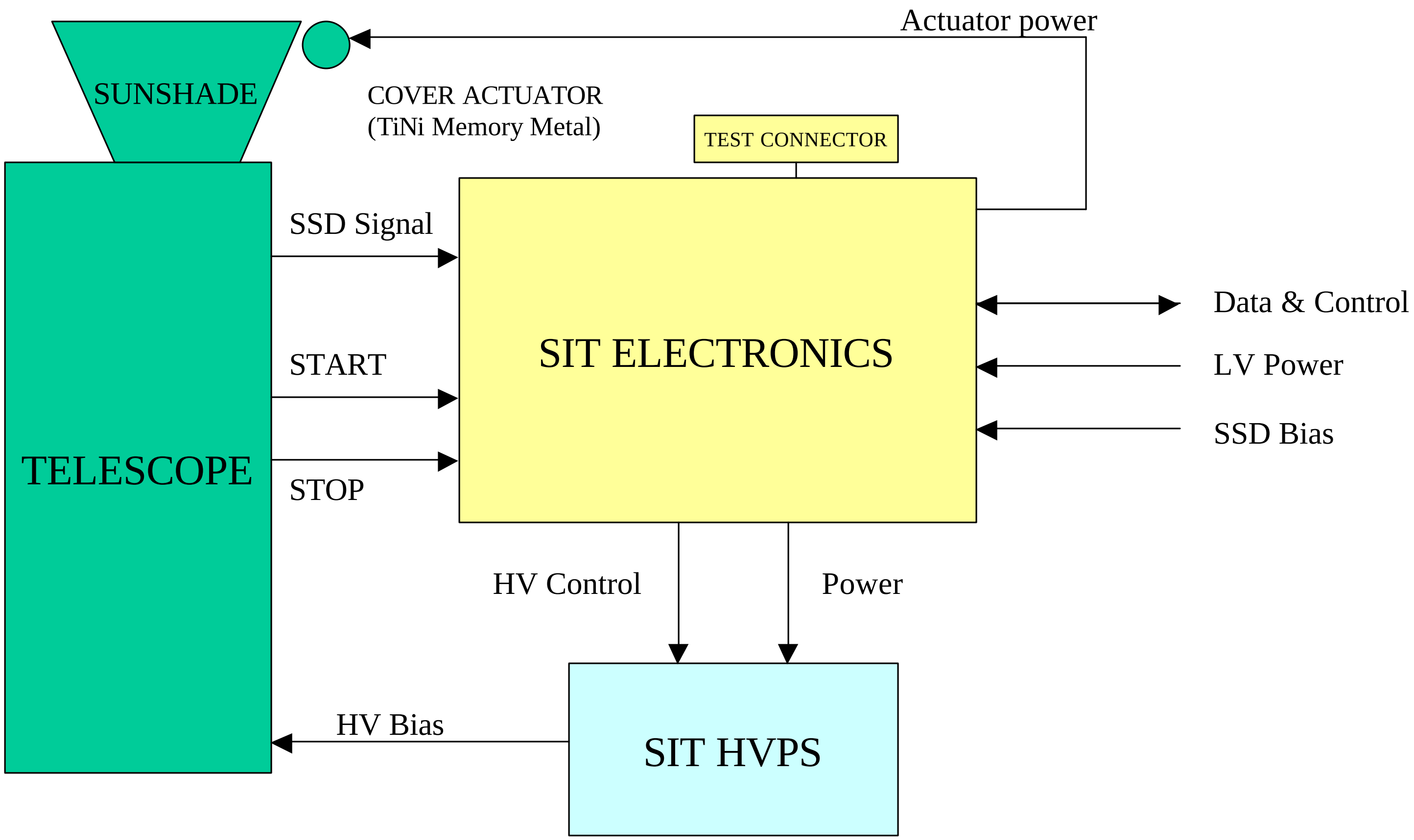
SIT OVERVIEW

- TOF vs Total E
- He-Fe
- 30keV/Nuc - 2 MeV/Nuc
- Resolve He^3 from He^4, C from O
- Single Telescope pointing near Parker spiral
  - 0.4 cm^2ster
  - 17 x 44 degree FOV
- SSD, MCPs, thin foils, HV bias supply
- Non-reclosable acoustic cover
- Heritage
  - Telescope, analog TOF electronics designs were flown on WIND/STEP
  - Energy electronics ASIC is descendant of design flown on ACE/ULEIS
  - HVPS design flown by UCB
  - Digital TOF and logic electronics designs are new

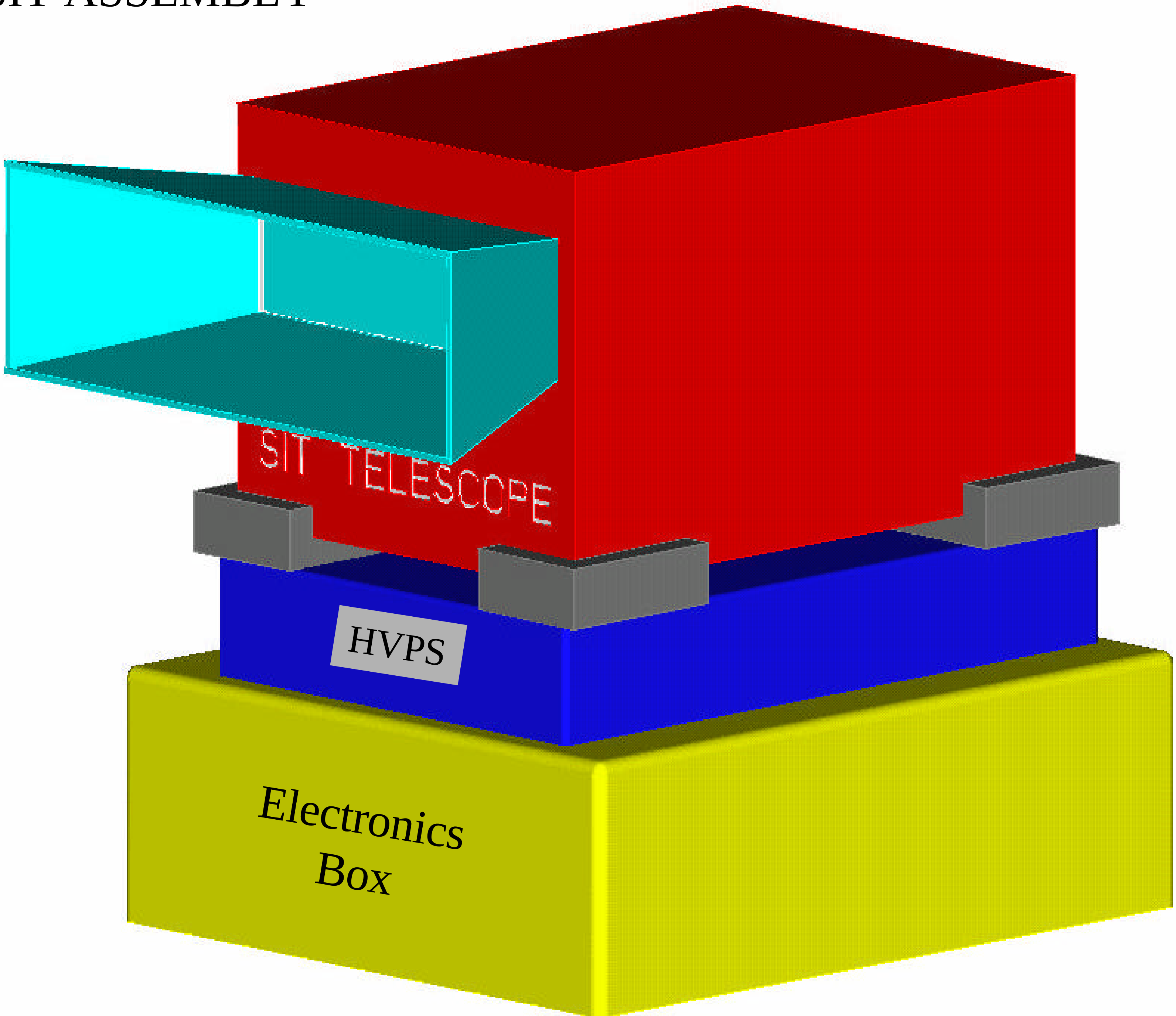
Requirement Verification

- FOV - verify mechanical design
- Energy - bench calibration, particle calibration at BNL
- Mass Resolution - alpha test in vacuum at UMd
- Energy Resolution - alpha test in vacuum at UMd
- Geometric Factor - verify mechanical design
- Background - vacuum test at UMd
- Max Event Rate - bench performance tests

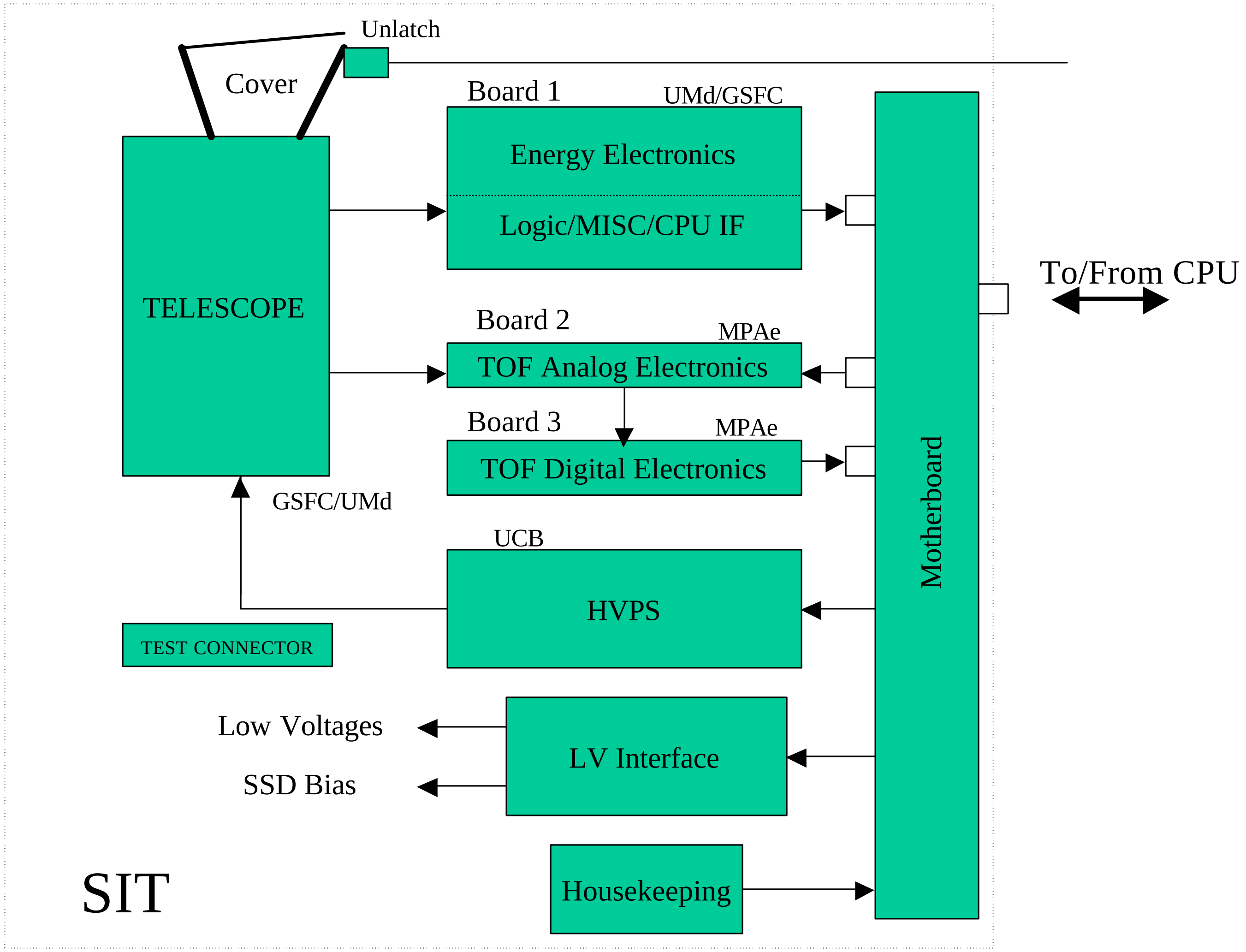
SIT - Box-Level Block Diagram



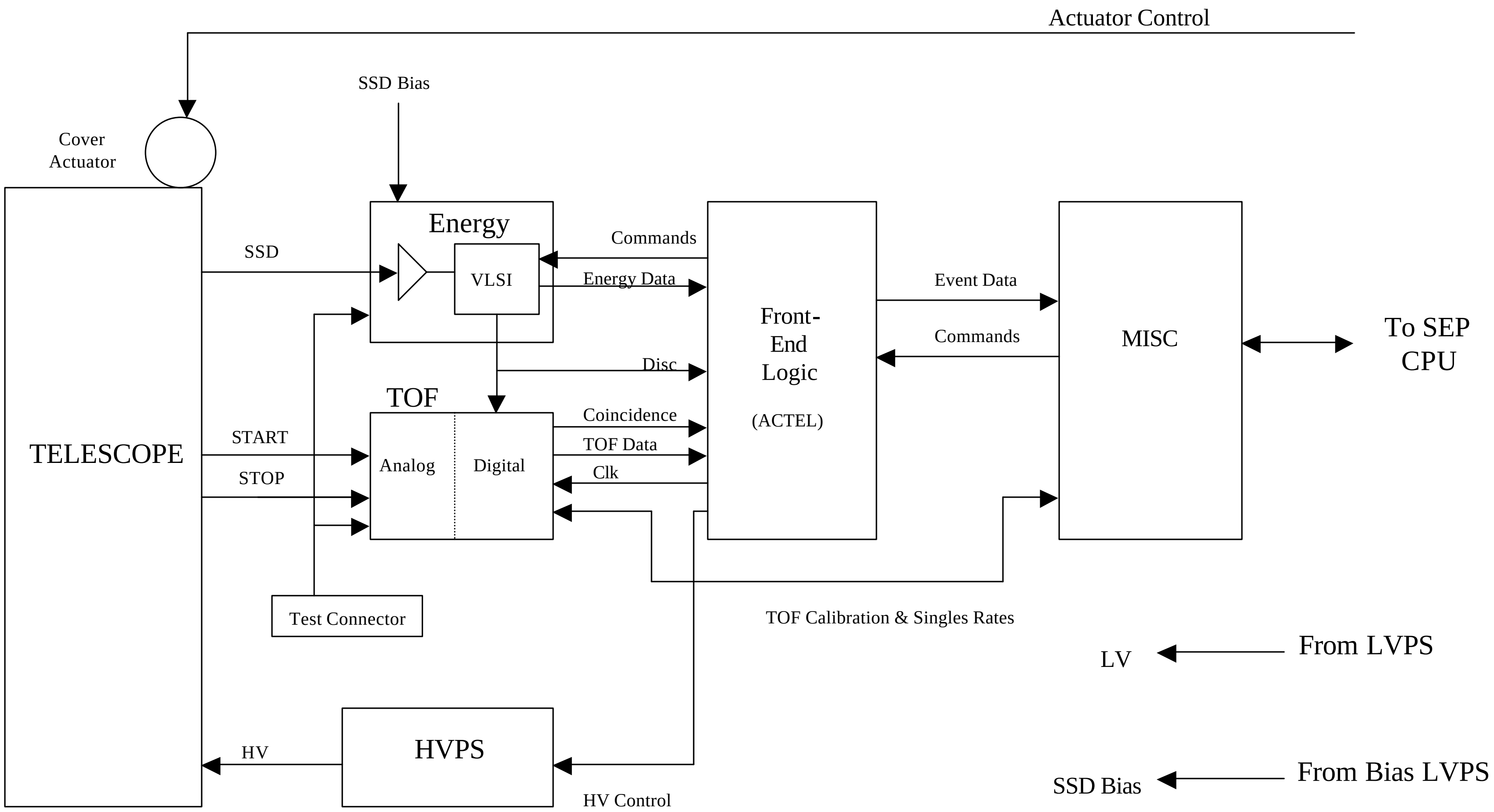
SIT ASSEMBLY



SIT Board Level Block Diagram



SIT FUNCTIONAL BLOCK DIAGRAM



SIT Development Plan

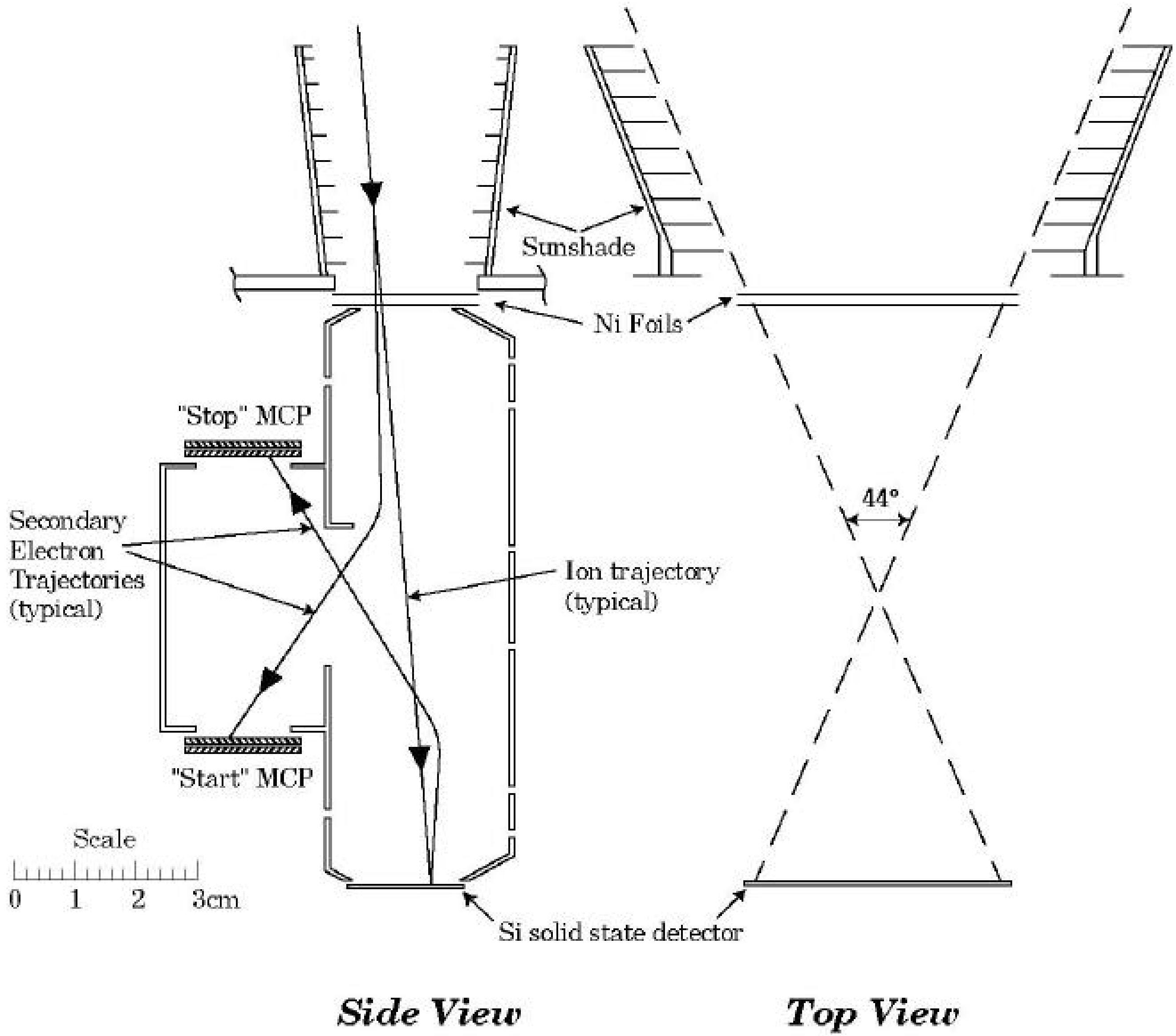
- <u>Telescope</u> - GSFC fabricate from existing UMd WIND designs with GSFC mechanical modifications to fit on STEREO. UMd provides SSDs, MCPs & foils.
- <u>Energy System</u> - Use Caltech VLSI chip with UMd CSA, GSFC designs control logic (integrated with Logic system) using UMd inputs. Fabrication at GSFC.
- <u>TOF System</u> - Provided by MPAe with inputs from UMd
- <u>Logic System</u> - GSFC, with inputs from UMd. On same board as Energy system.
- <u>HVPS</u> - Provided by UCB from UMd specification
- <u>Housings/Mechanical Design/Thermal</u> - GSFC
- <u>Board and Unit Level Testing</u> - UMd
- For details see "Who Does What" below

Telescope

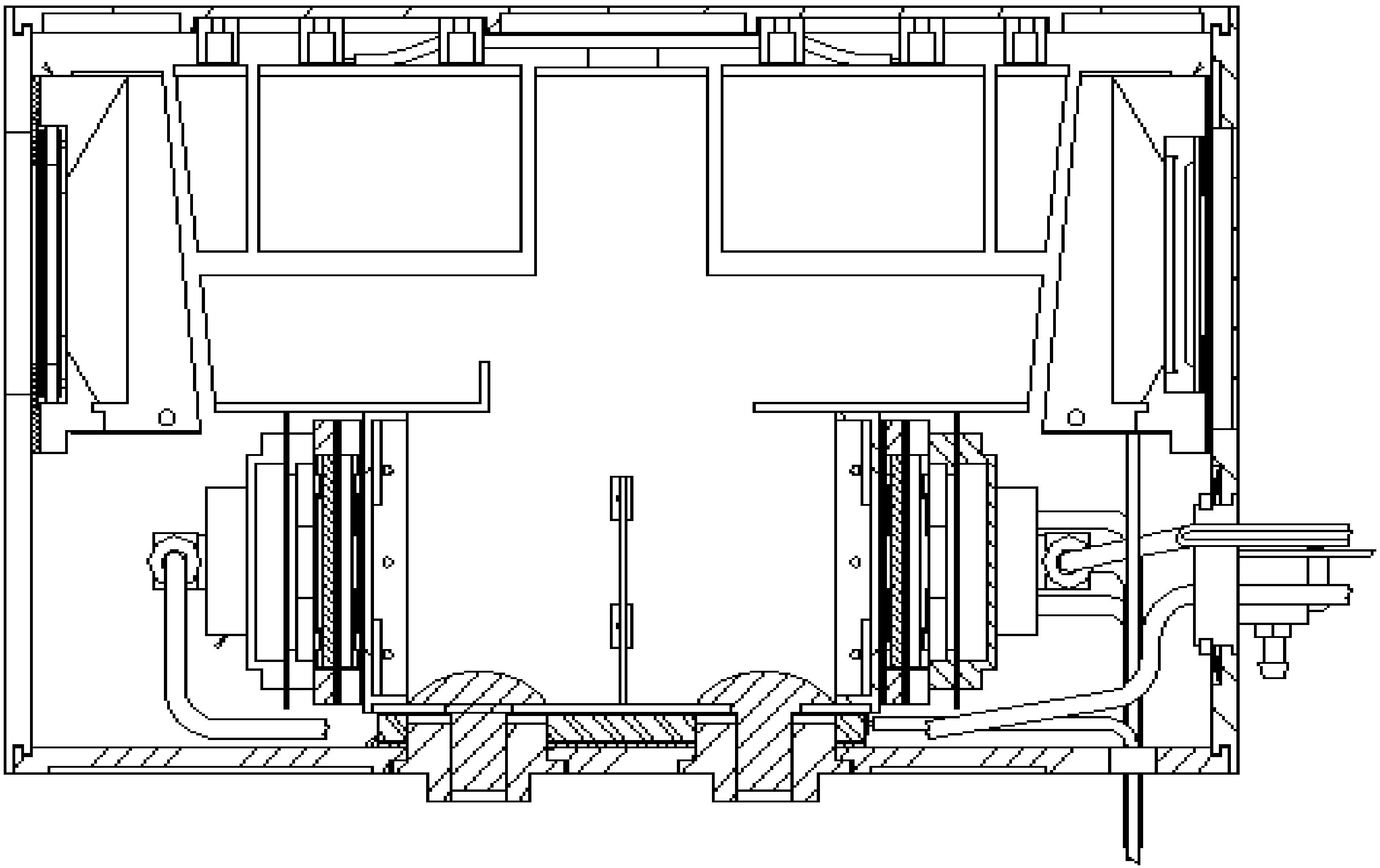
Telescope

- TOF vs E
- Energy - 1 SSD
  - Perkin Elmer (formerly Ortec) Si surface barrier
  - 15mm x 40 mm
  - 500u
  - bias ~150v
- TOF - 1 START & 1 STOP
  - 10 cm flight path
  - Burle (formerly Galileo) chevron pair micro-channel plates
  - ~1000v bias per plate, commandable
- Foils - 2
  - Lebow Corporation
  - Ni
  - 1000A, on grid

Suprathermal Ion Telescope (SIT)

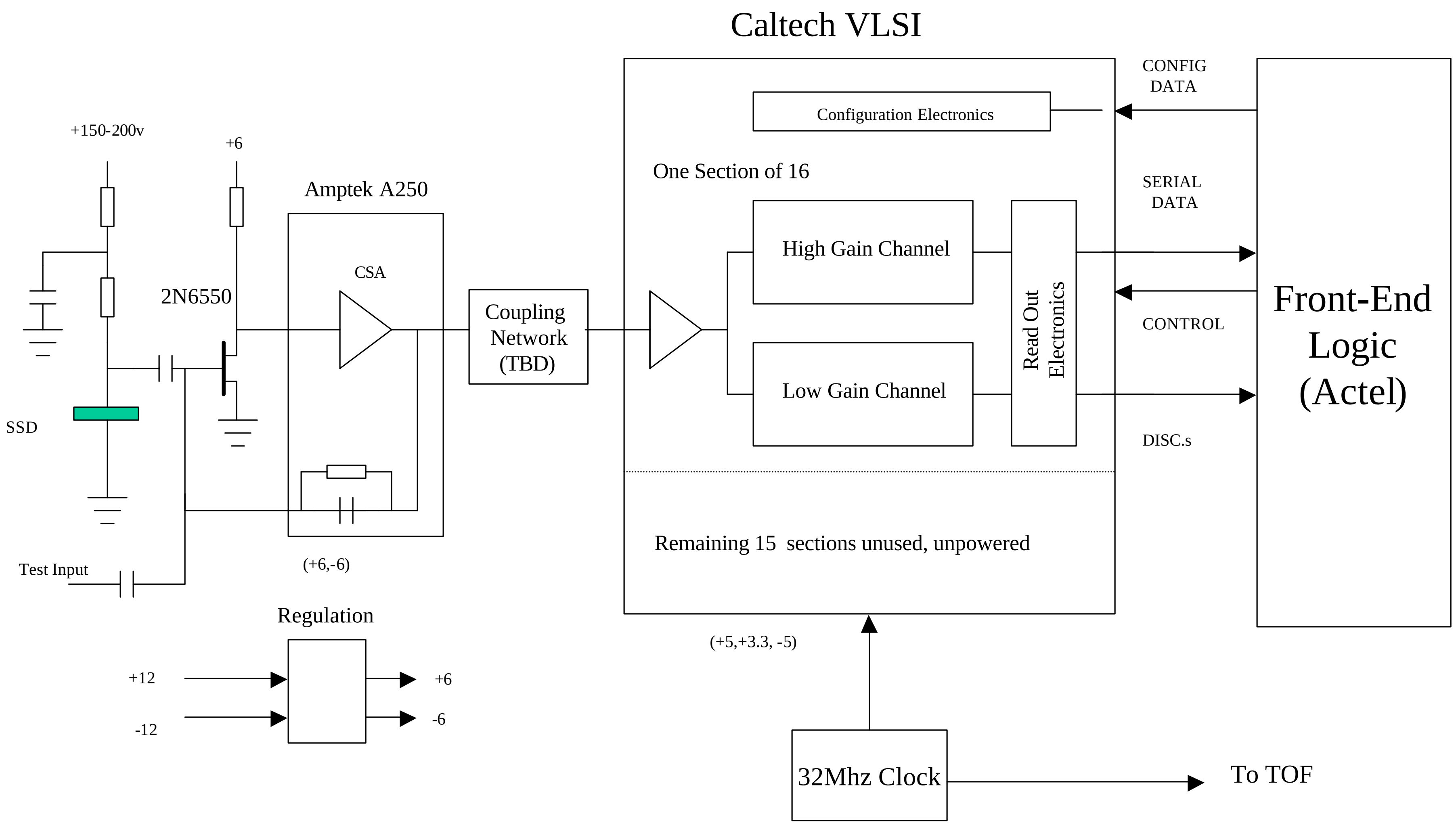


SIT Telescope Cross Section

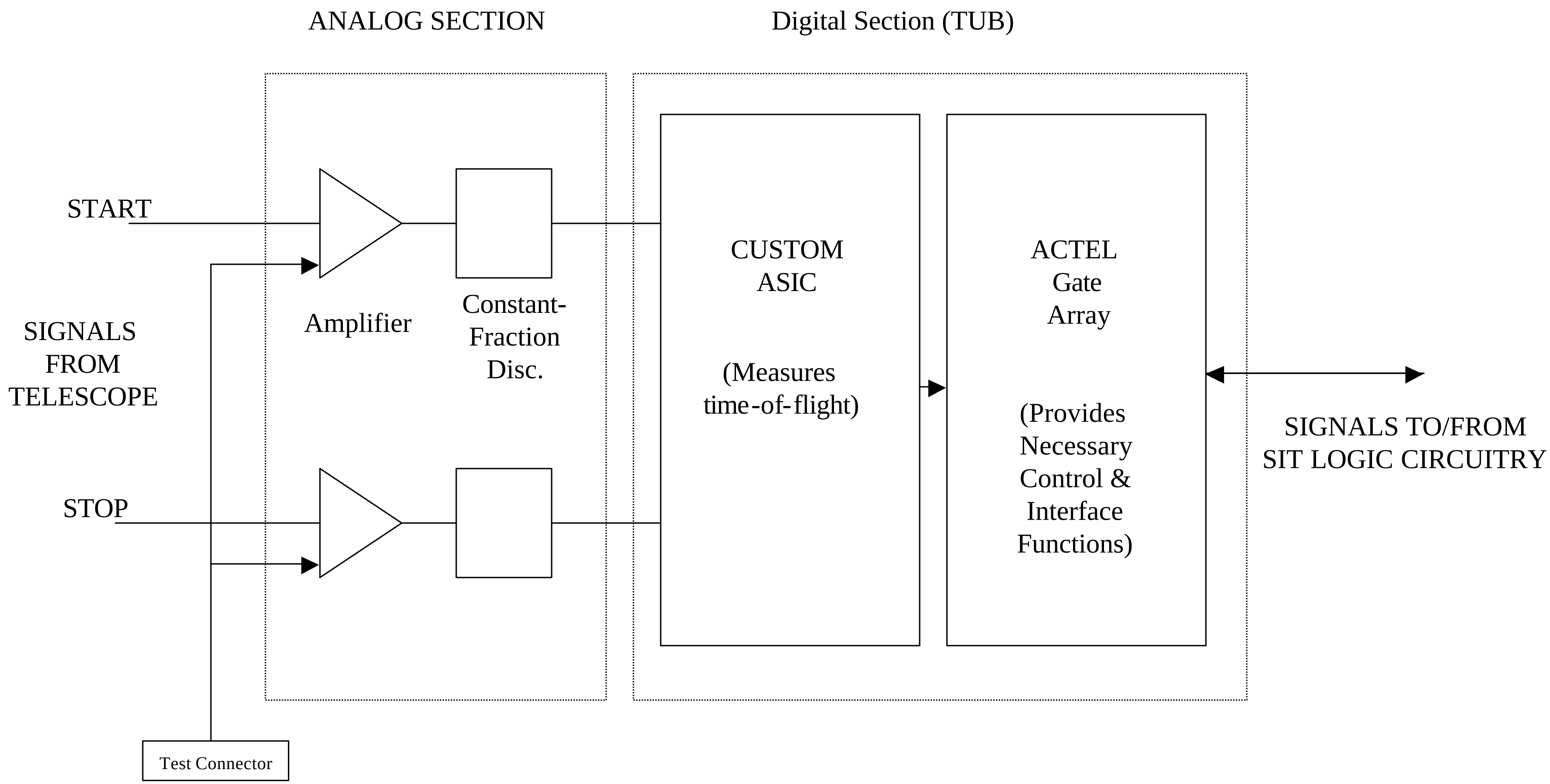


Electronics

SIT ENERGY SYSTEM BLOCK DIAGRAM

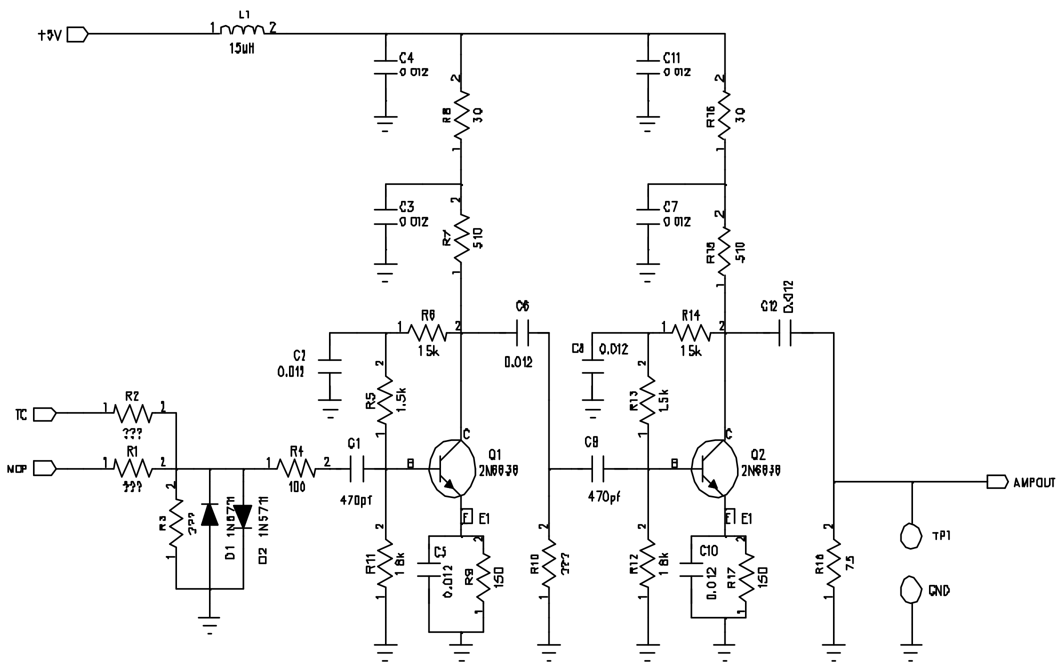


SIT TOF BLOCK DIAGRAM



6	5	4	3	2	1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

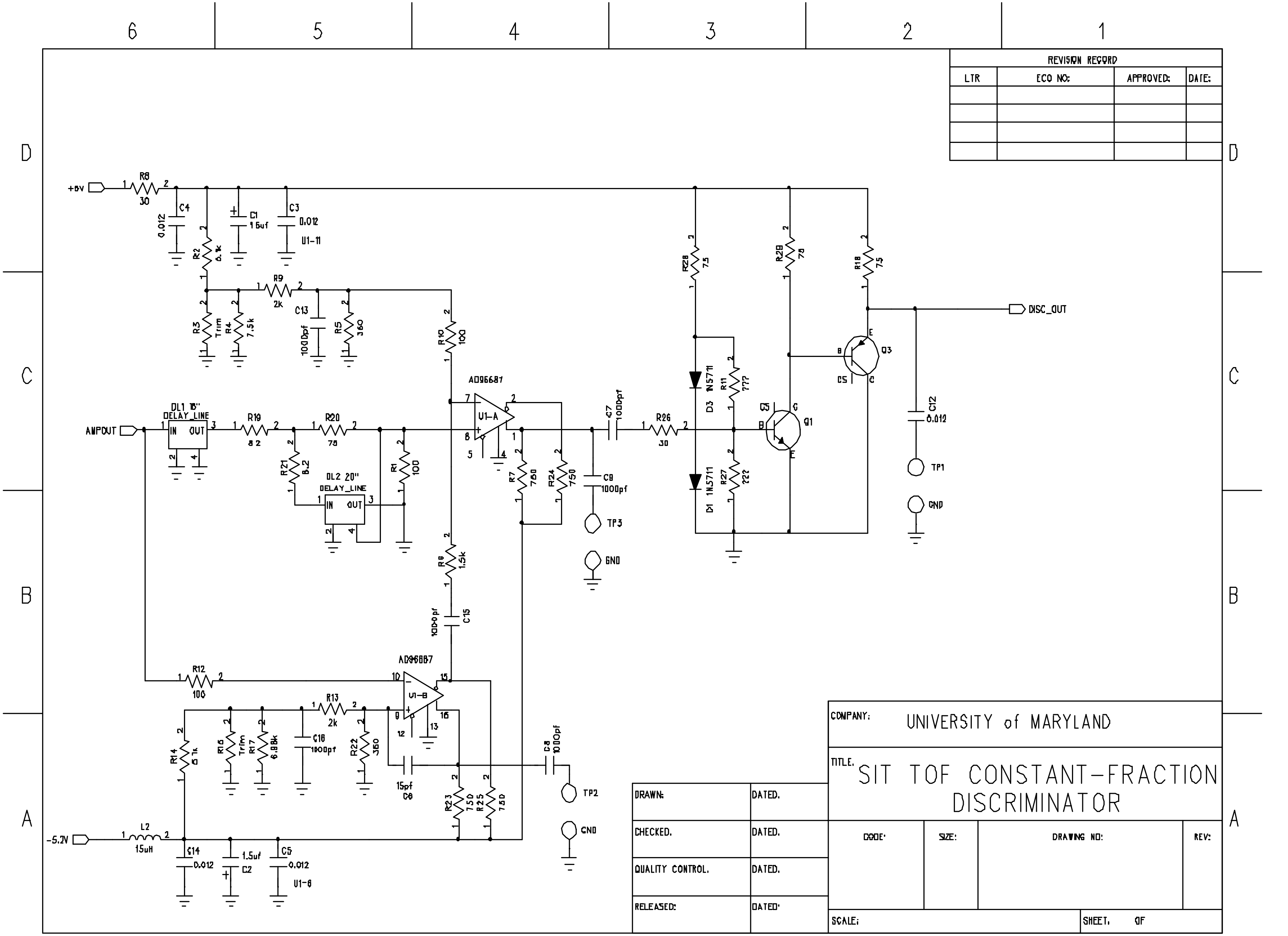


COMPANY.	UNIVERSITY of MARYLAND
TITLE	SIT TOF AMPLIFIER

DRAWN.	DATED.
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED.	DATED.

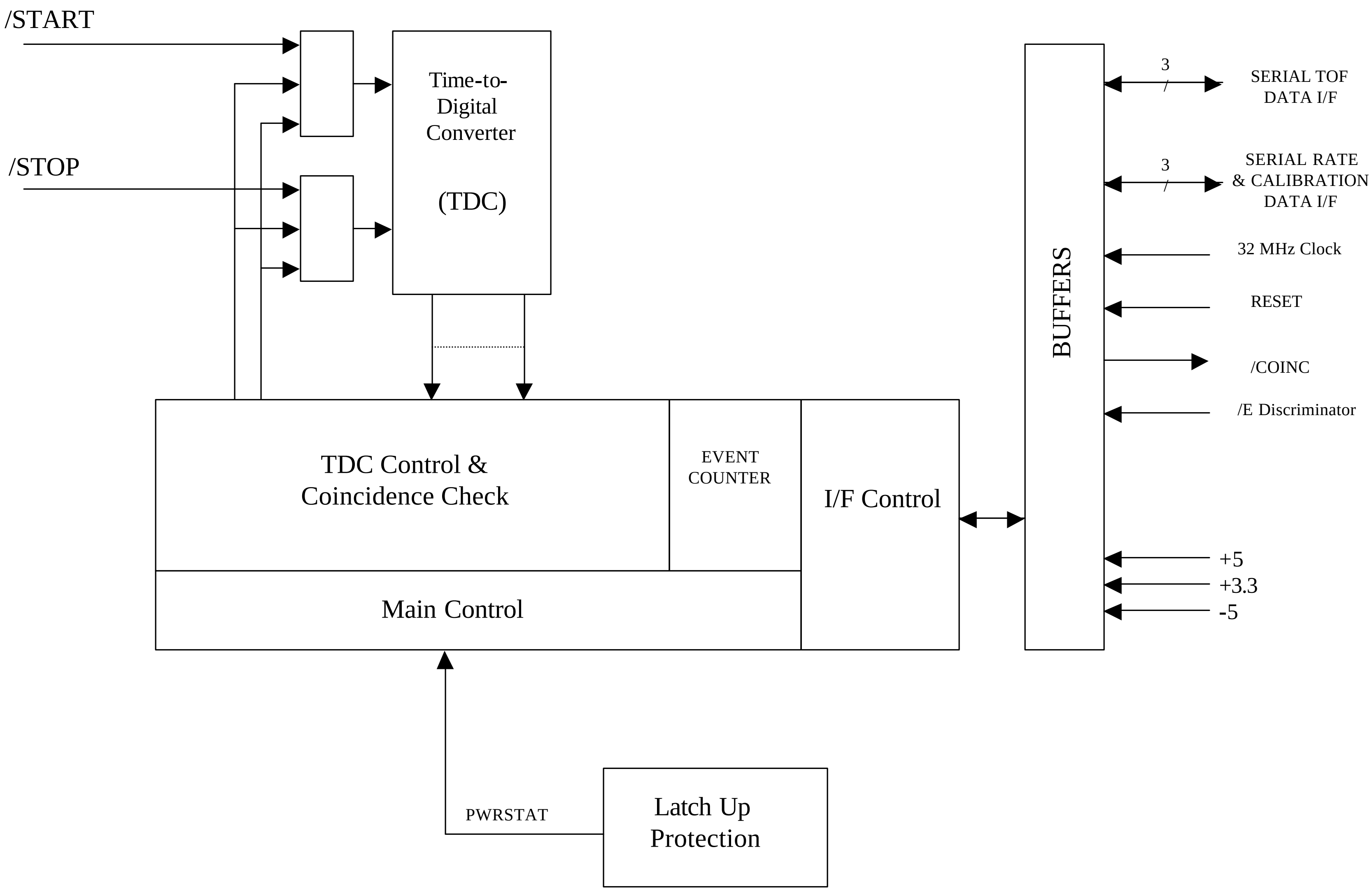
CODE.	SIZE:	DRAWING NO:	REV.

SCALE: SHEET: OF



REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+5V
R8
30
C4
0.012
C1
15uf
C3
0.012
U1-11
R2
R9
2k
R3
Trim
R4
7.5k
C13
1000pf
R5
360
R10
100
AD96687
U1-A
DL1 15"
DELAY_LINE
IN
OUT
AMPOUT
R19
82
R20
75
R21
8.2
DL2 20"
DELAY_LINE
R1
100
R7
750
R24
750
C7
1000pf
C9
1000pf
TP3
GND
R26
30
R28
75
R29
75
R18
75
D3 1N5711
D1 1N5711
R11
R27
Q1
Q3
DISC_OUT
C12
0.012
TP1
GND
R6
1.5k
C15
1000pf
AD96687
U1-B
R12
100
R13
2k
R14
R15
Trim
R17
6.88k
C16
1000pf
R22
360
15pf
C6
C8
1000pf
TP2
GND
R23
750
R25
750
-5.2V
L2
15uH
C14
0.012
1.5uf
C2
C5
0.012
U1-6
COMPANY: UNIVERSITY of MARYLAND
TITLE: SIT TOF CONSTANT-FRACTION DISCRIMINATOR
DRAWN:
DATED.
CHECKED.
DATED.
QUALITY CONTROL.
DATED.
RELEASED:
DATED:
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET.
OF

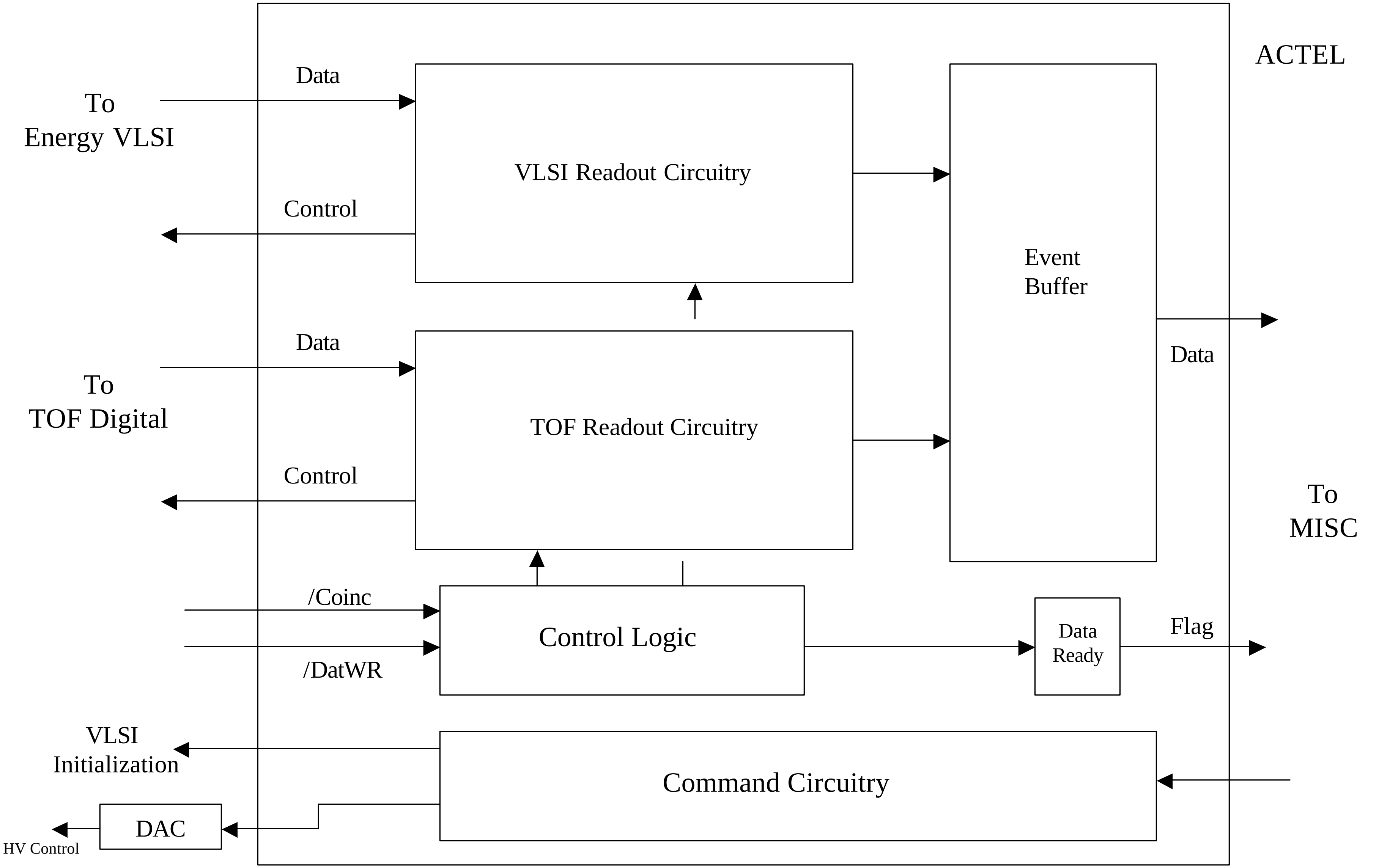
TOF DIGITAL BLOCK DIAGRAM

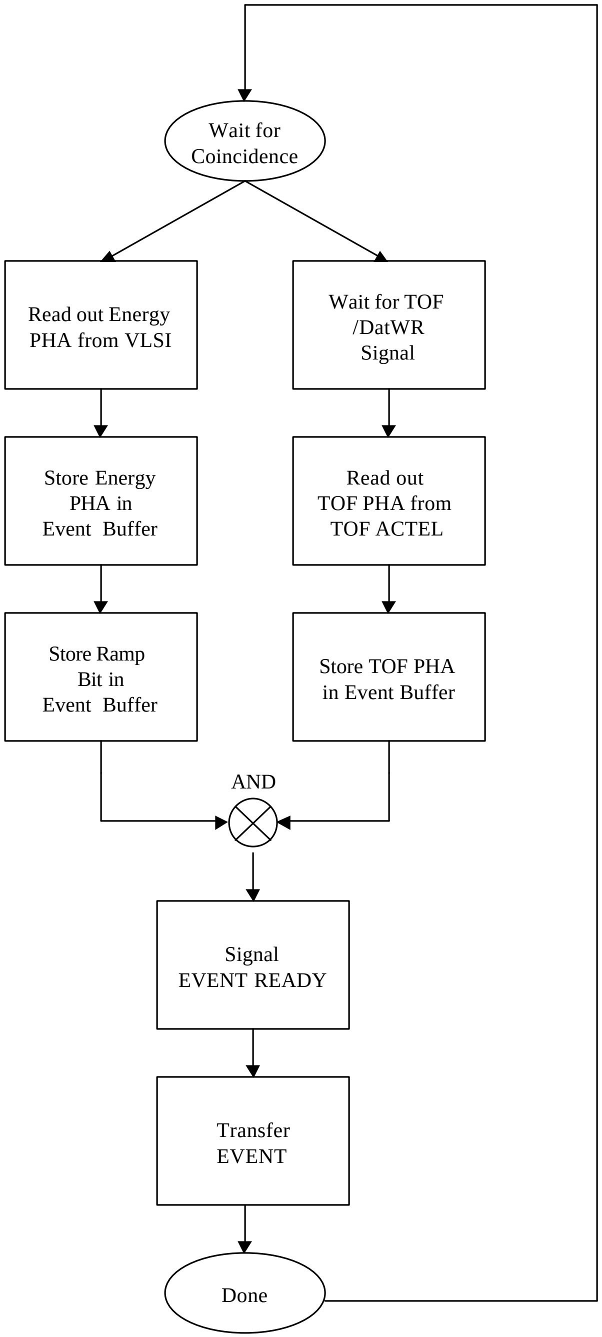


Front-End Logic Tasks

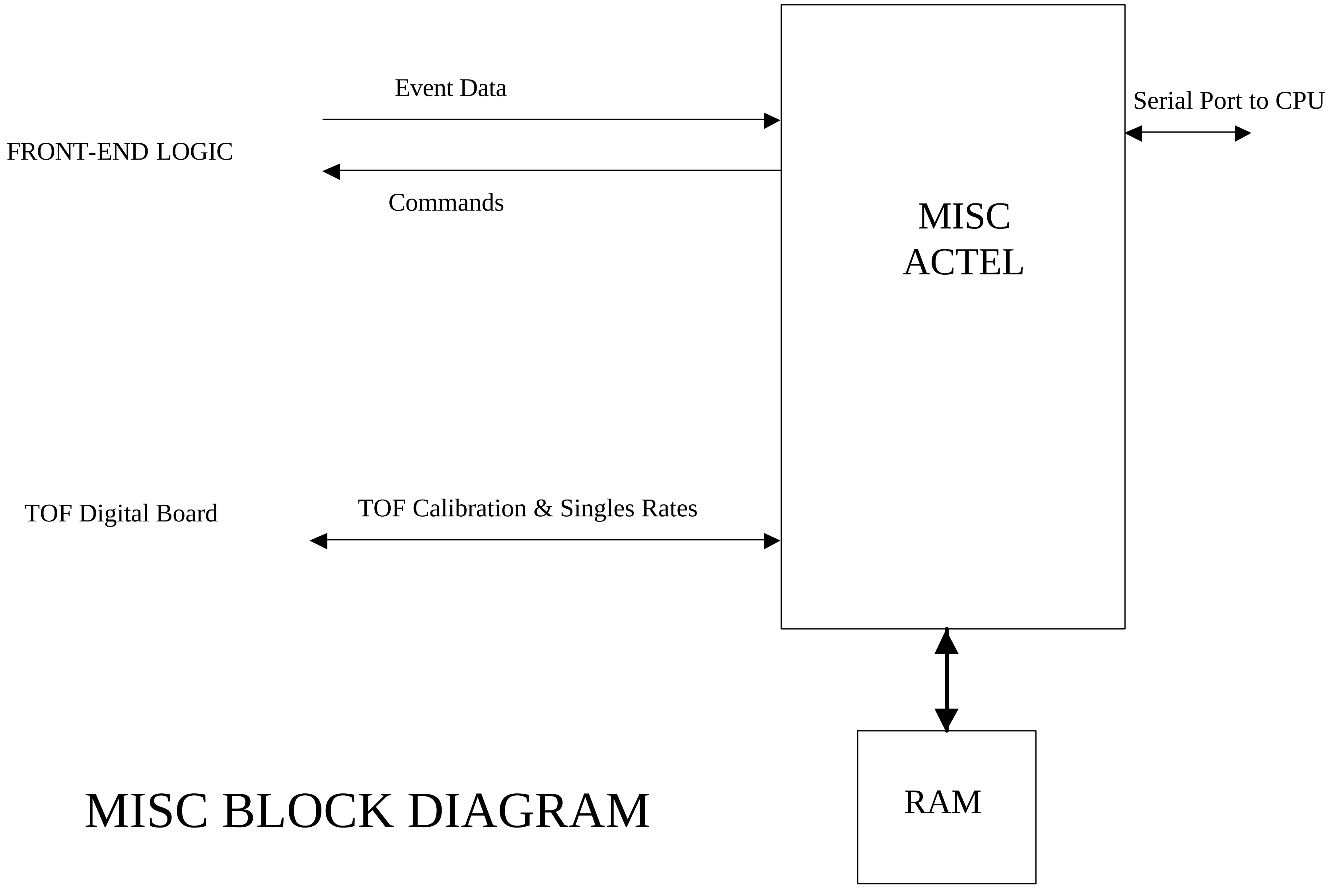
- Collect Events and present them to MISC
- Receive Commands from MISC and Execute them
  - VLSI initialization and control
  - HV control (Digital to Analog conversion)

SIT Front-End Logic ACTEL





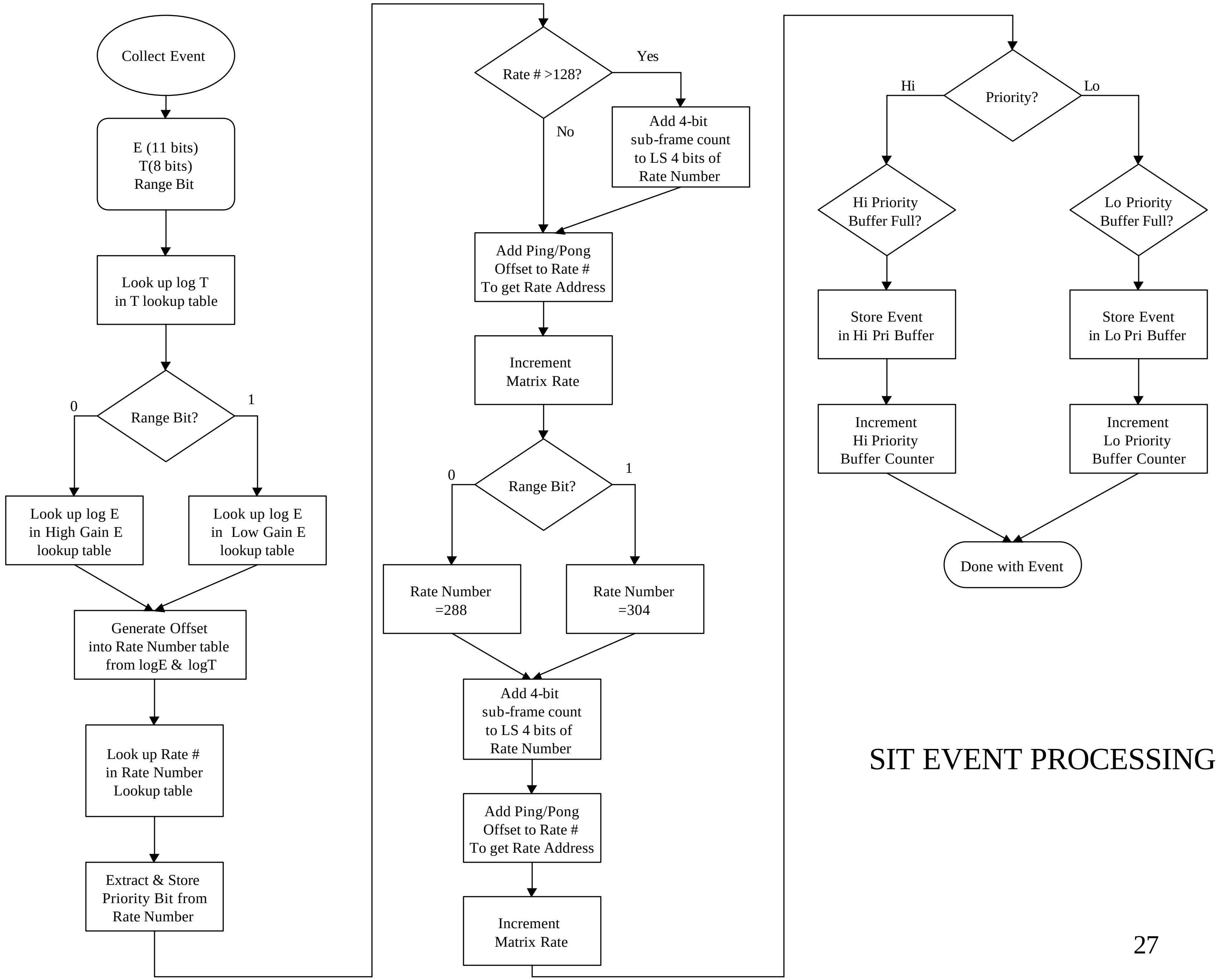
SIT Event Pre-Processing in Front-End Logic



MISC BLOCK DIAGRAM

MISC Tasks

- Initialization of Self and VLSI
  - Power-on reset
  - External reset from SEP CPU
  - Watchdog timer?
- Event Processing
  - Event binning/matrix rate counting
  - Event prioritization and storage
- TOF Calibration
- Singles Rate Collection (counting done in TOF)
- Digital status word
- Command Processing
- Output data Formatting and Transmitting
  - rate compression
  - buffer management
  - output data to SEP CPU

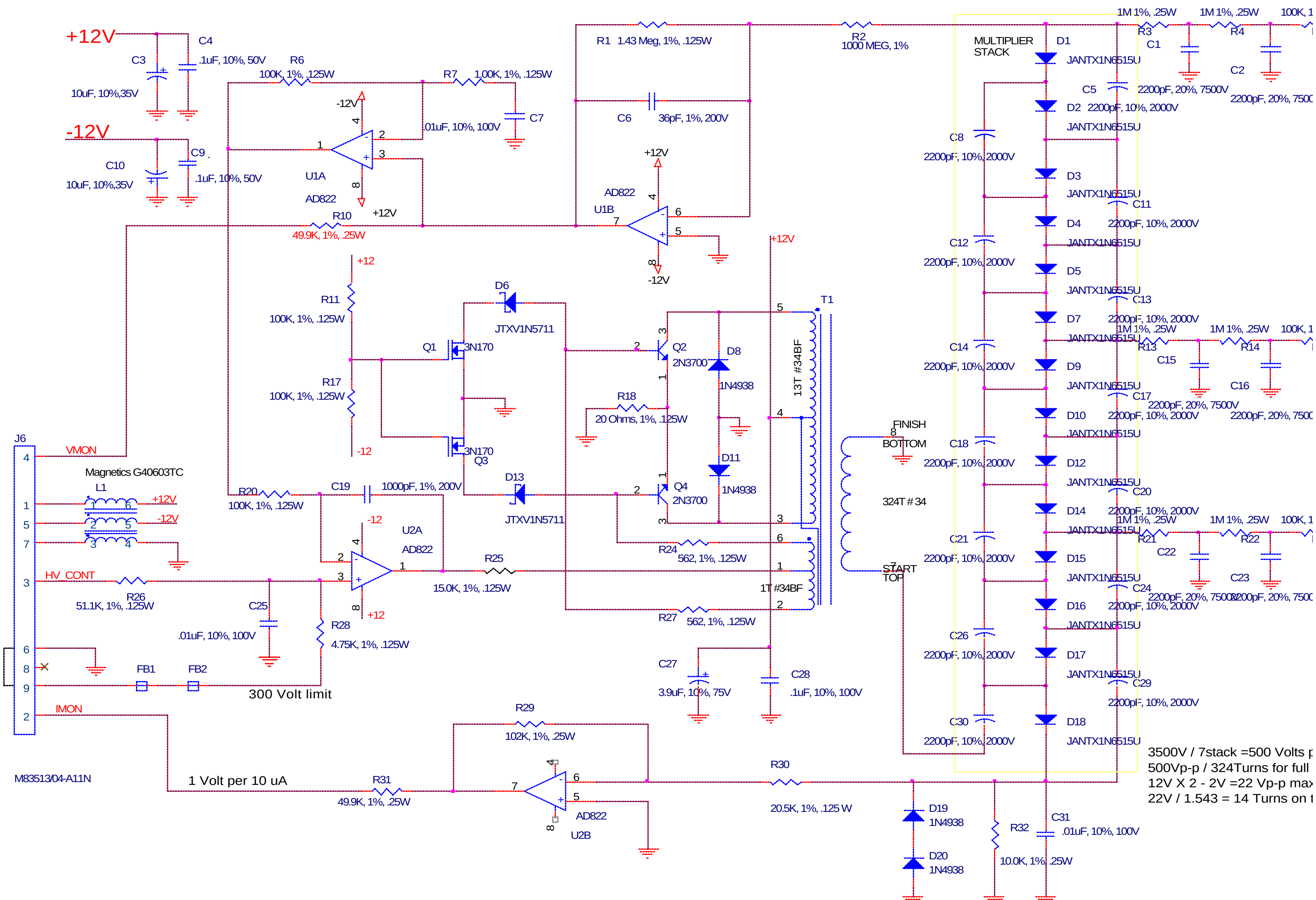


SIT EVENT PROCESSING

HVPS

- Provides bias voltages to operate the microchannel plates and to “focus” the secondary electrons produced by incoming ions
- Nominal voltages: 3400,3200,2200,2000,1000 and 950 v
- Top voltage controlled by command, others change proportionally
- 0-5v control voltage
- Maximum output ~4200v
- On/Off Command : 5v level
- Disable plug to prevent operation during ground testing
- Operates on +/- 12v
- Supplied in housing by UCB

HVPS Schematic (UCB)



at 40ua and 3500 volts, the output consumption is 140 mW

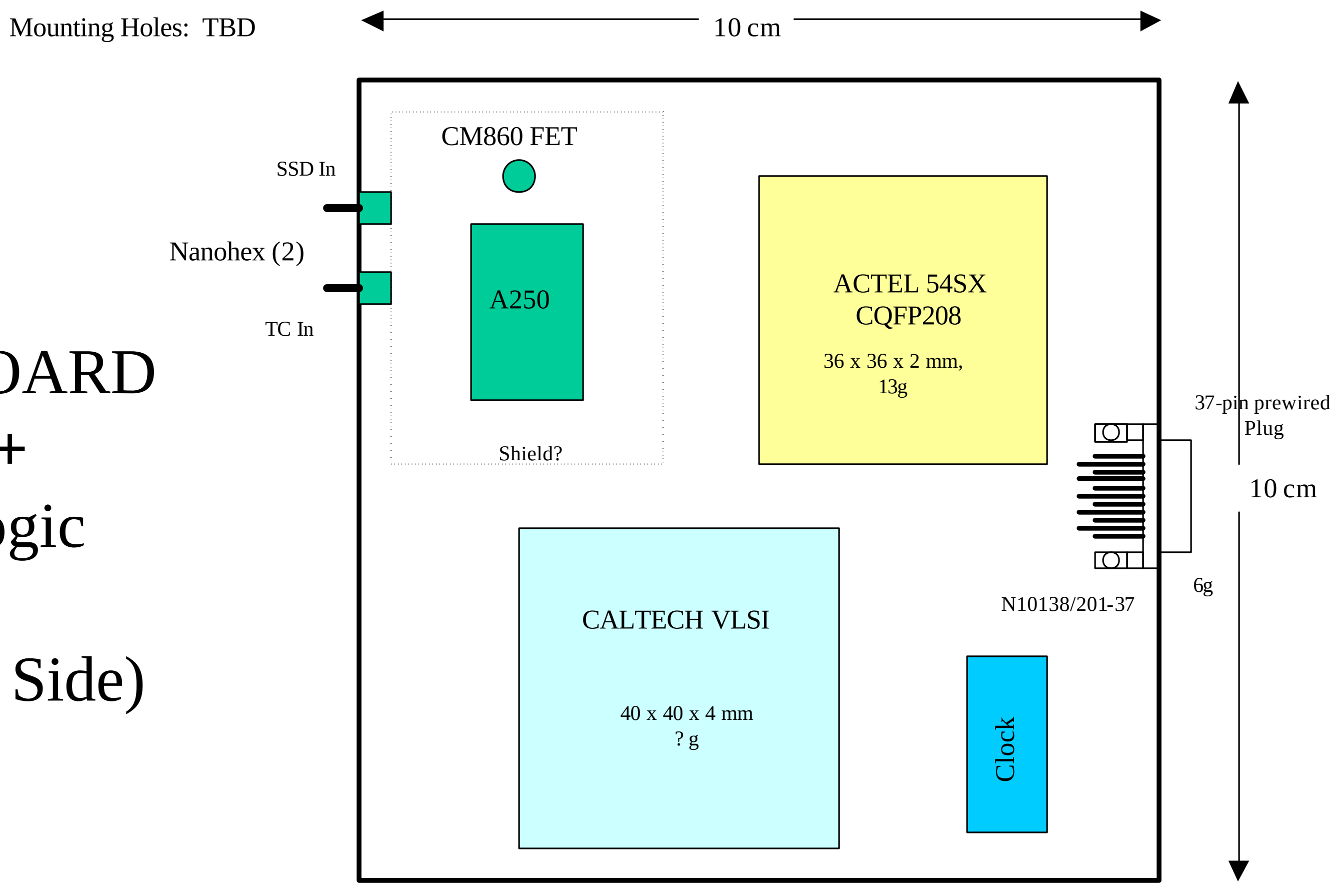
Housekeeping/Status

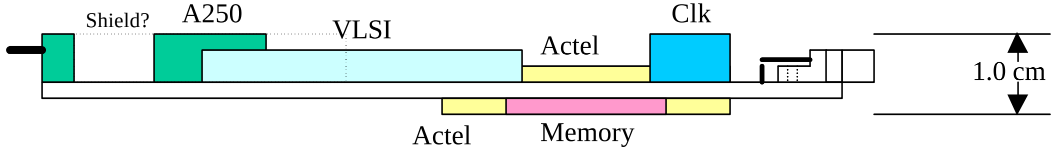
- AD590 (2) for temperature monitoring
  - TOF board (likely warmest spot)
  - Telescope SSD (most sensitive to temperature)
  - HV Monitor
- Digital status word maintained in MISC and read out with data

Board Layouts

E BOARD + Logic

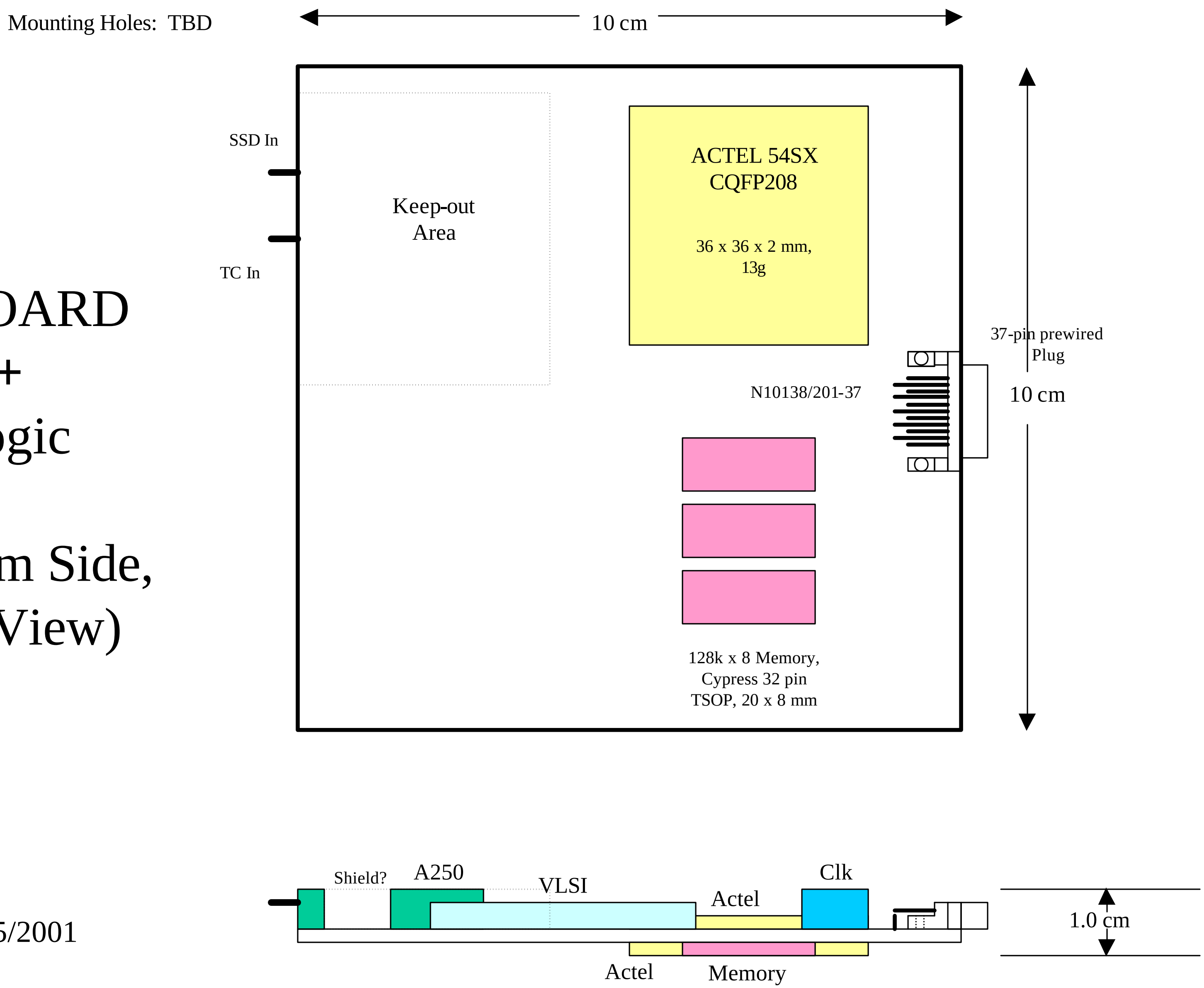
(Top Side)



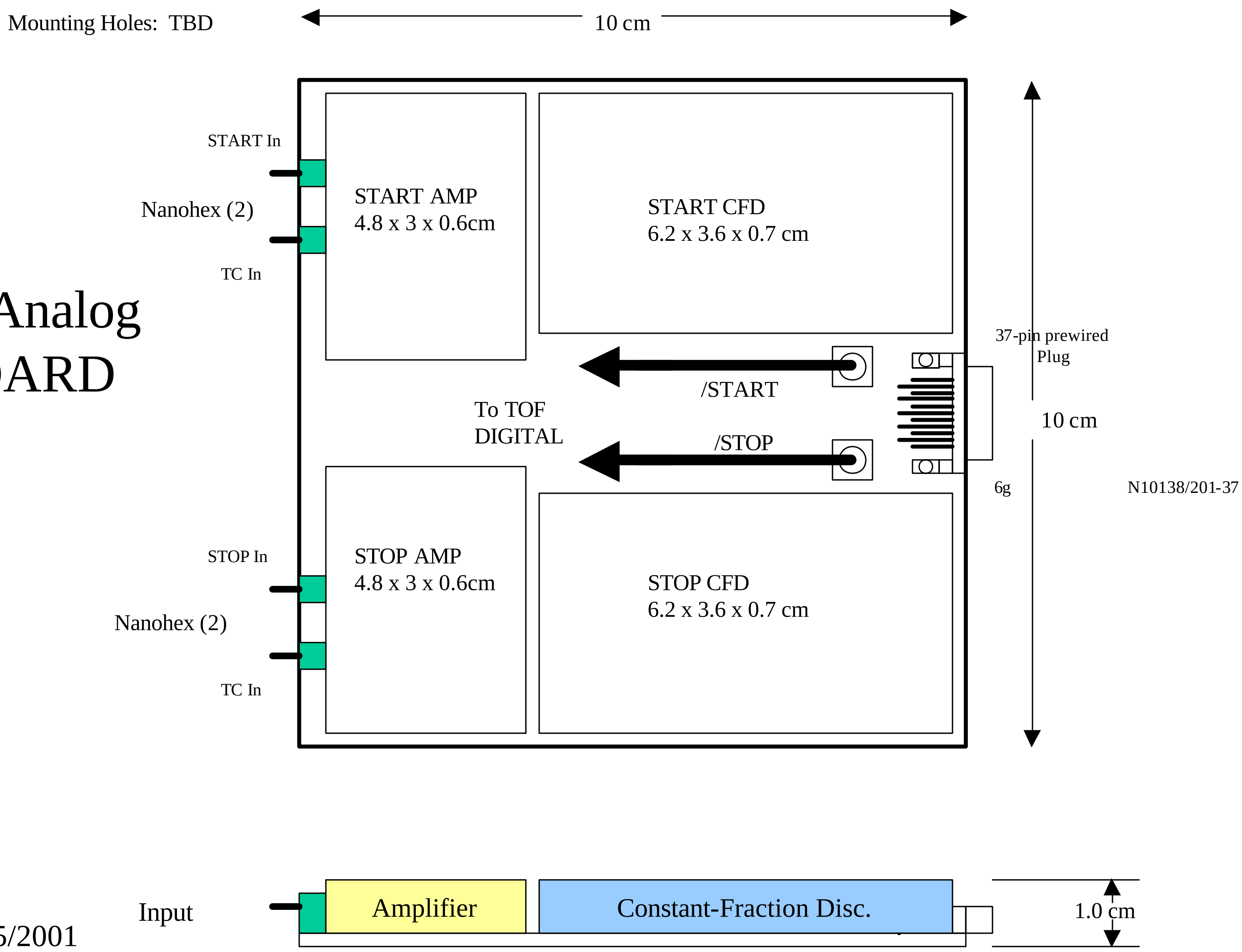


E BOARD
+
Logic

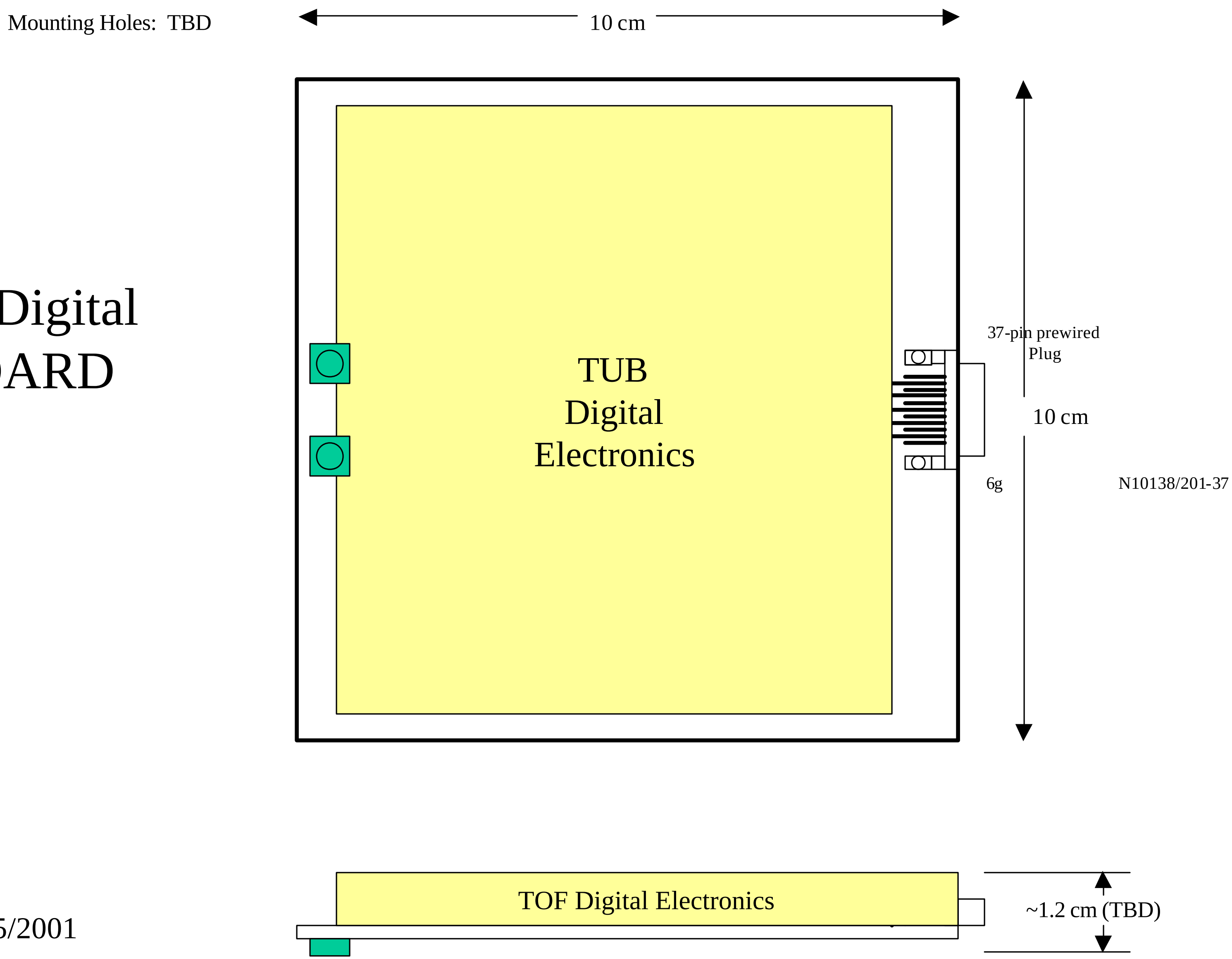
(Bottom Side, Top View)

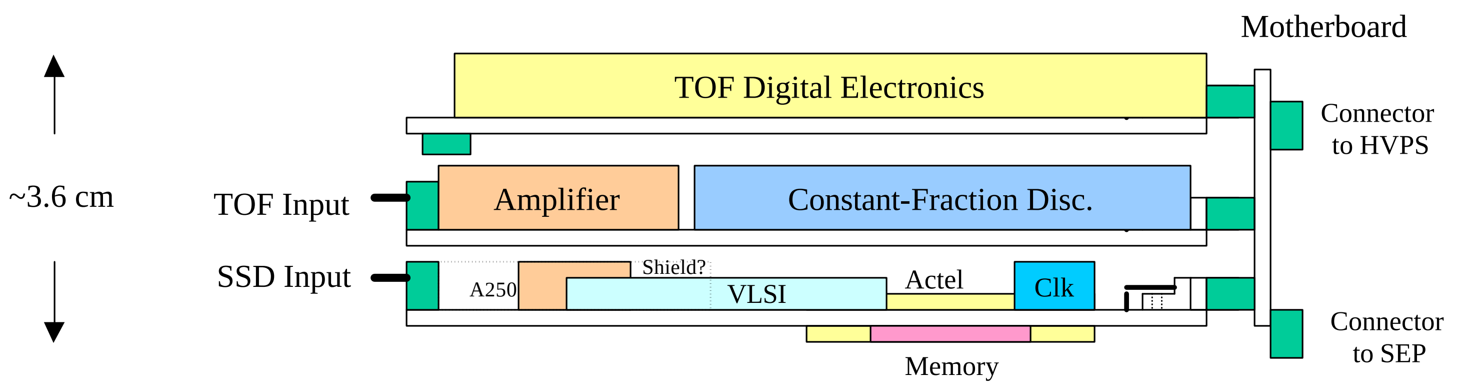


TOF Analog BOARD



TOF Digital BOARD





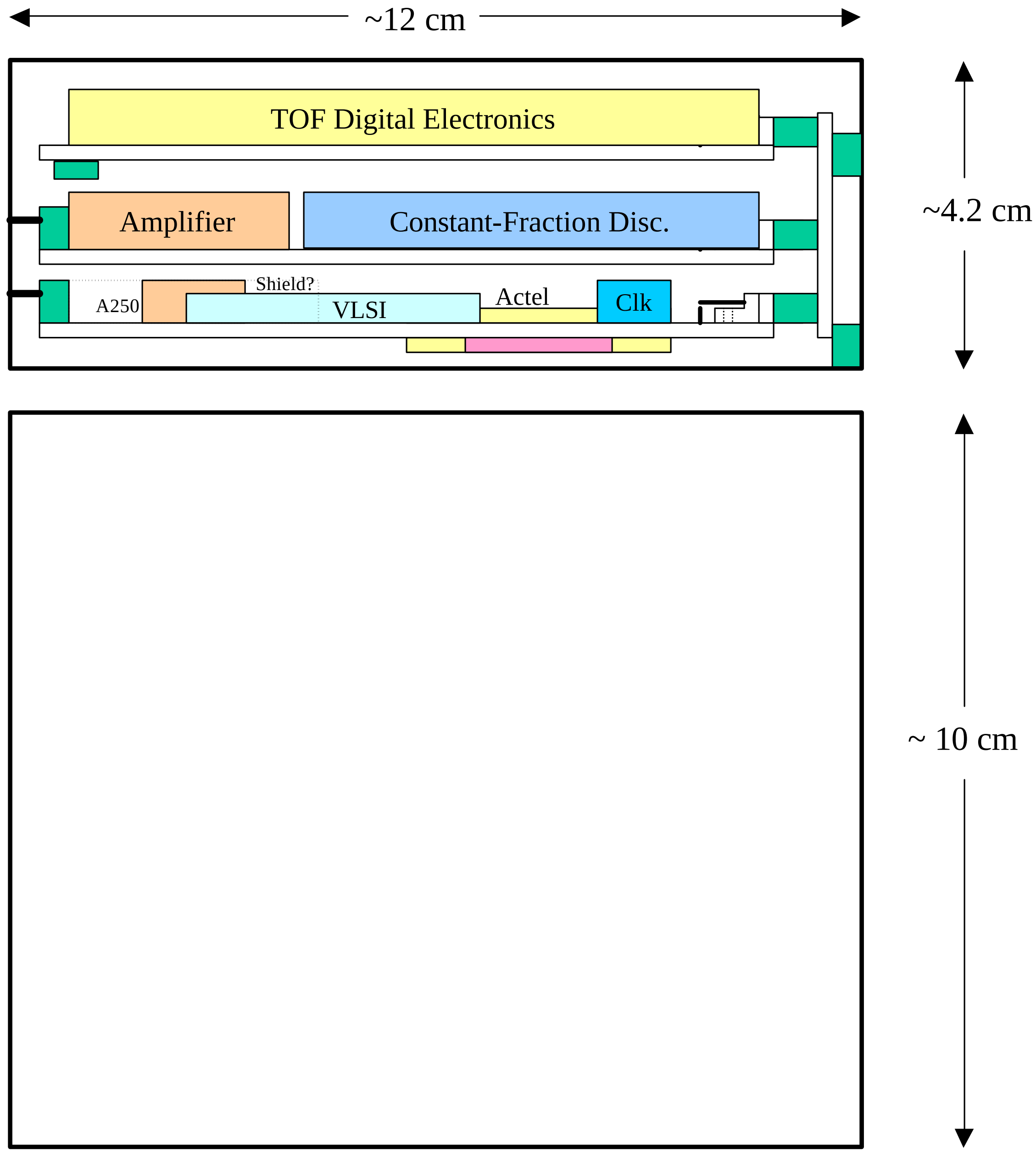
SIT Electronics Assembly

MOTHER BOARD

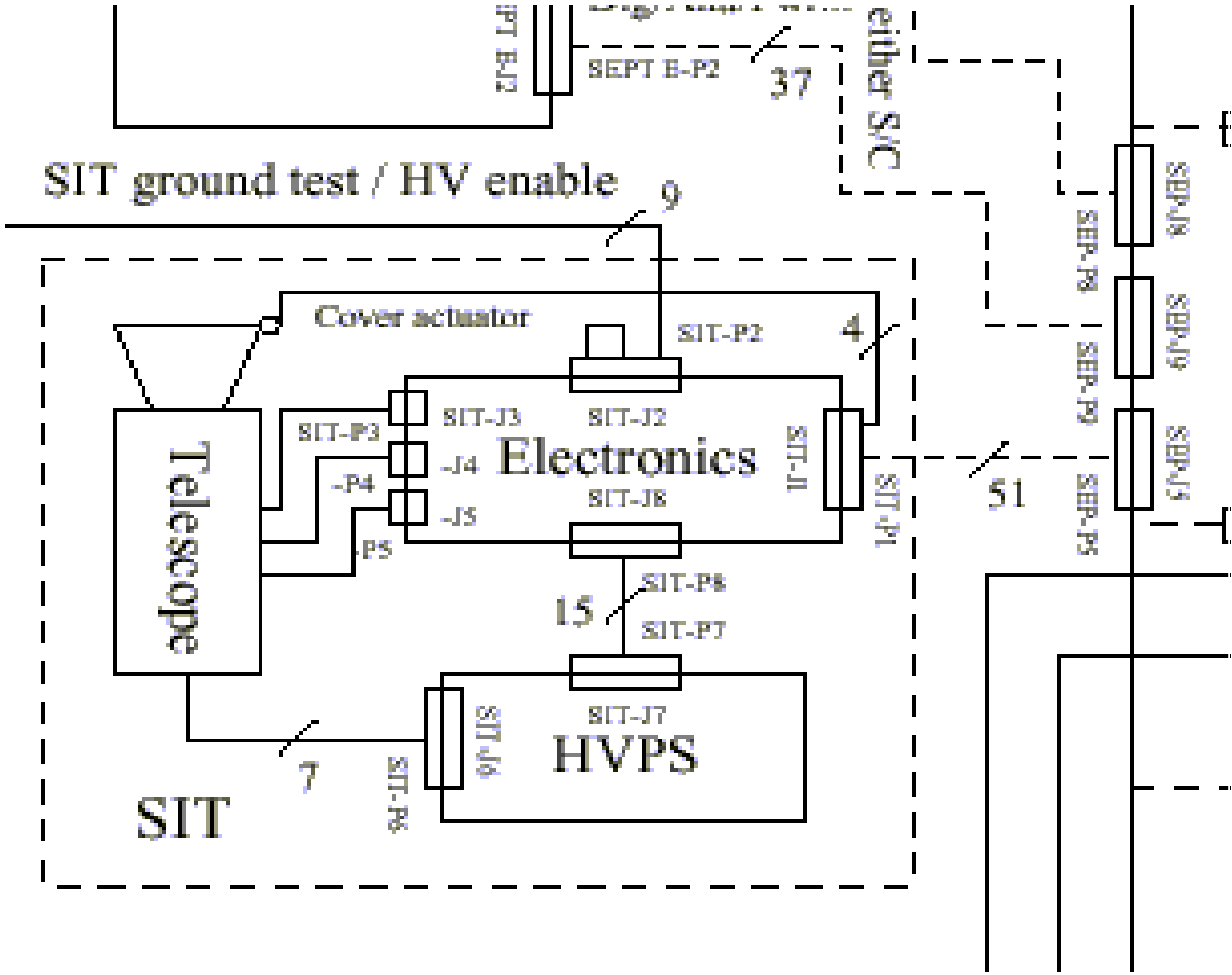
Overall Size

Side View

TOP View



Cabling


SEPT E-P2
37
either S/C
SIT ground test / HV enable
9
Cover actuator
SIT-P2
4
SIT-J3
SIT-J2
SIT-P3
-J4
Electronics
-P4
-J5
SIT-J8
-P5
SIT-J1
SIT-P1
51
SIT-P8
15
SIT-P7
SIT-J7
HVPS
SIT-J6
SIT-P6
7
Telescope
SIT
SEP-J8
SEP-P8
SEP-J9
SEP-P9
SEP-J5
SEP-P5

Data

Data Overview

- Data types
  - PHA Events
  - Rates
  - Housekeeping
  - Status
- Collected and processed in MISC
- Buffered in MISC and sent to SEP CPU
- CPU adds analog HK data, organizes, packetizes and passes on to IDPU.

Data Types - PHA

- PHA Events - 32 bits
  - Energy (11 bits + ramp bit)
  - TOF (8 bits)
  - Matrix rate number (7 bits)
  - priority/state (2 bits)
  - time within record (3 bits)

Data Types - Rates

- Rates
  - discriminator - counted in digital TOF circuit
    - START, STOP, E(ramp0), E(ramp1), VS, Event
  - matrix - classification of events by mass and energy in MISC
    - high time resolution (3-5 minutes) 9 rates
    - low time resolution (~15 minutes) 128 rates

Data Types - Other

- Housekeeping
  - temperatures
    - AD590s (2)
  - hv monitor
- Digital Status
  - details TBD

Data Organization

- Data will be organized into Science Records of TBD minutes, containing all the PHA, rate, status and HK data for that period. This association of data allows convenient processing on the ground.

- Commands will be synchronized to change instrument state at the beginning of a science record

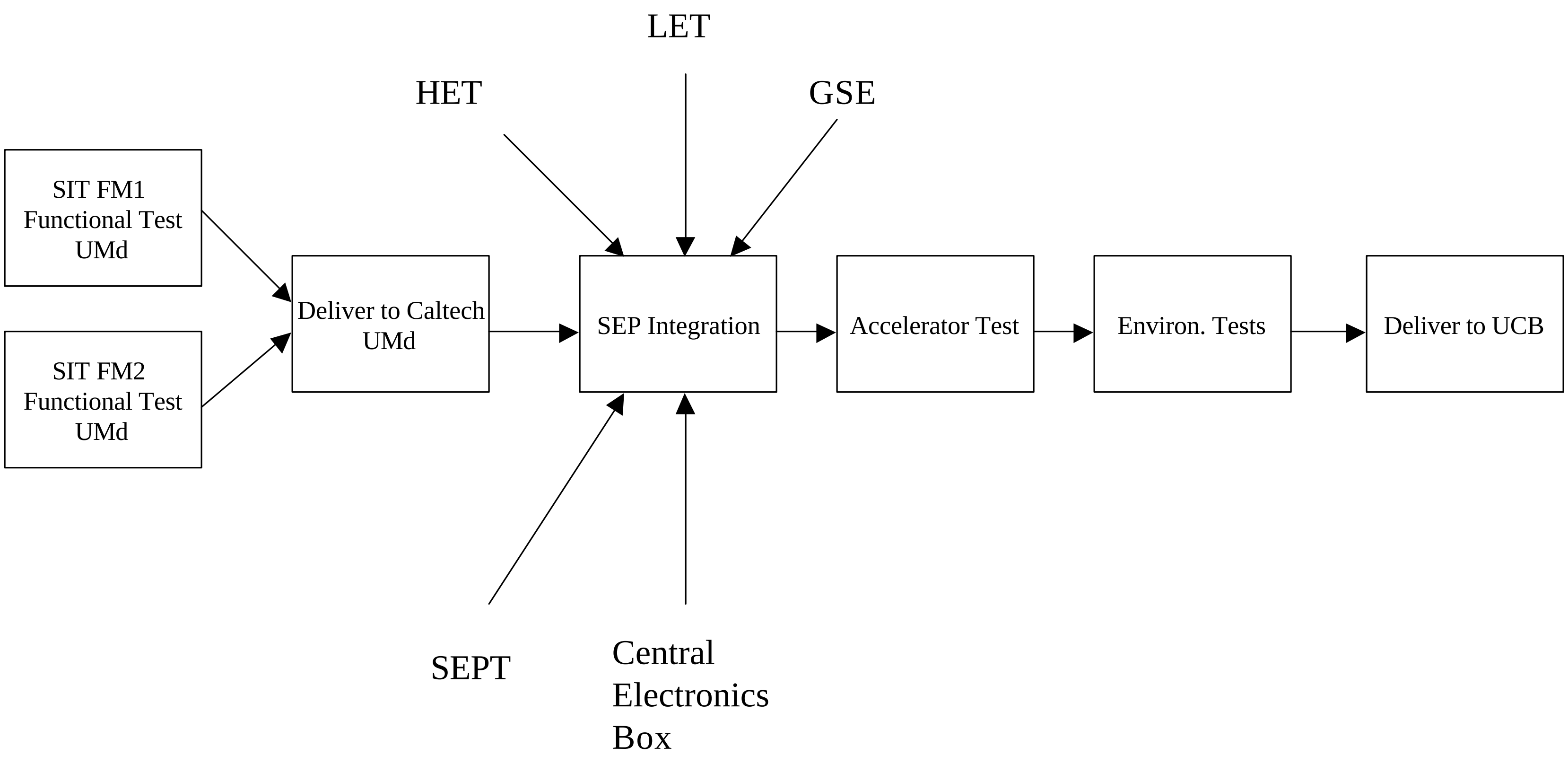
- Details are still being worked out

Bit Rate

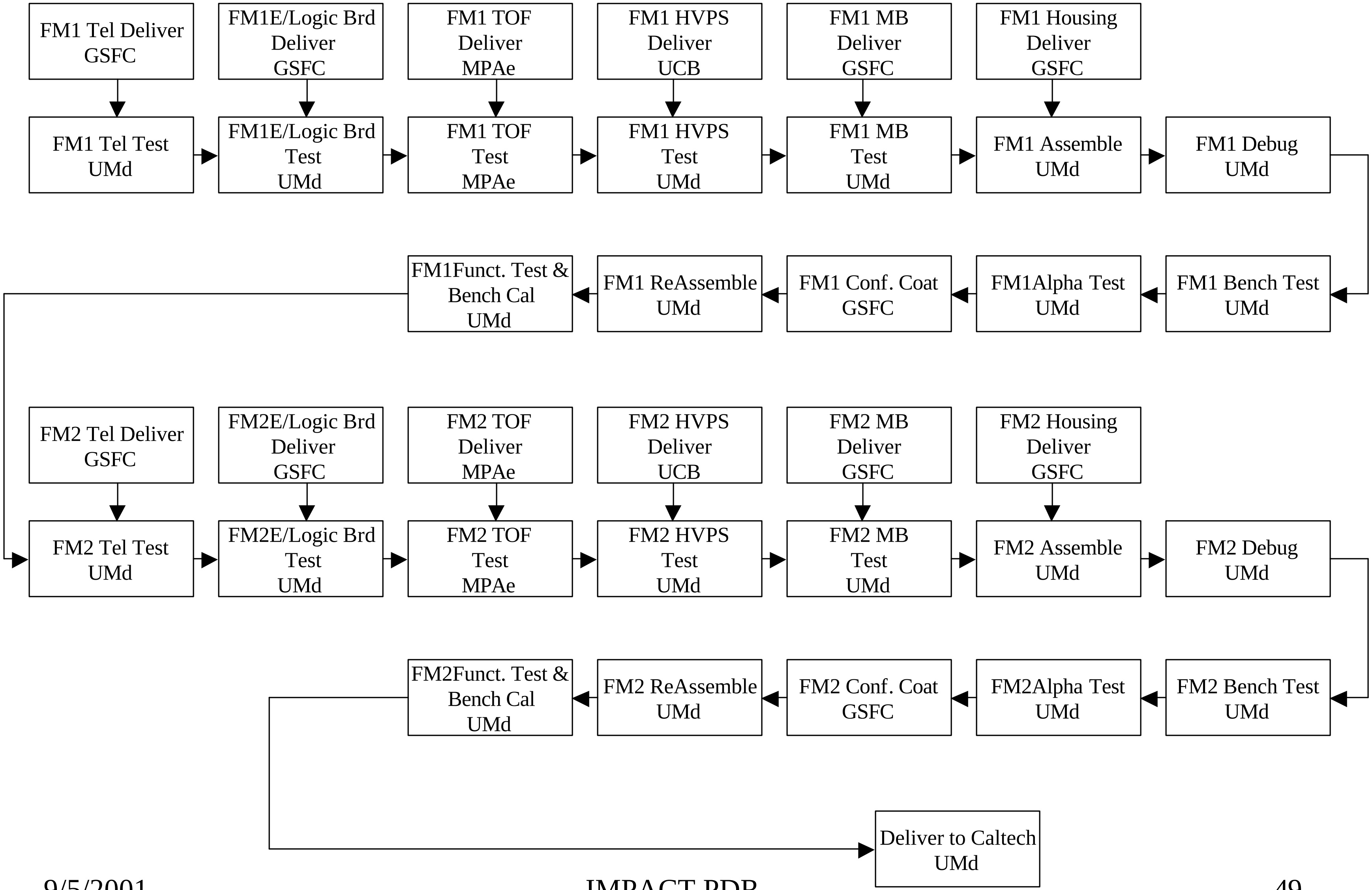
- Assigned Bit Rate - 240 bps
- Usage - being worked out but a typical scenario is:
  - Science Record period = 15 minutes = 27000 bytes
  - PHA events - 25,740 bytes
    - 7.15 events/sec @ 4 bytes/event
  - Matrix rates - 914 bytes
    - low time resolution, 128 rates, 5 min resolution, 12 bits
    - high time resolution, 9 rates, 1 min resolution, 12 bits
  - Discriminator rates - 240 bytes
  - HK - 60 bytes
    - 4 items, 1 minute resolution, 8 bits
  - Status - 30 bytes
  - Overhead - 16 bytes

Instrument

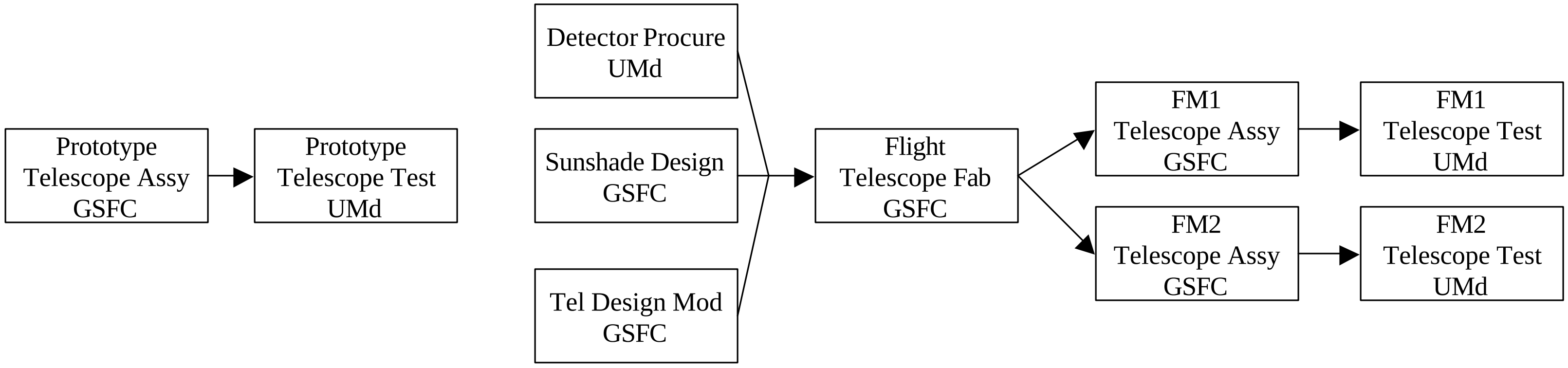
SEP Flow


LET
HET
GSE
SIT FM1 Functional Test UMd
SIT FM2 Functional Test UMd
Deliver to Caltech UMd
SEP Integration
Accelerator Test
Environ. Tests
Deliver to UCB
SEPT
Central Electronics Box

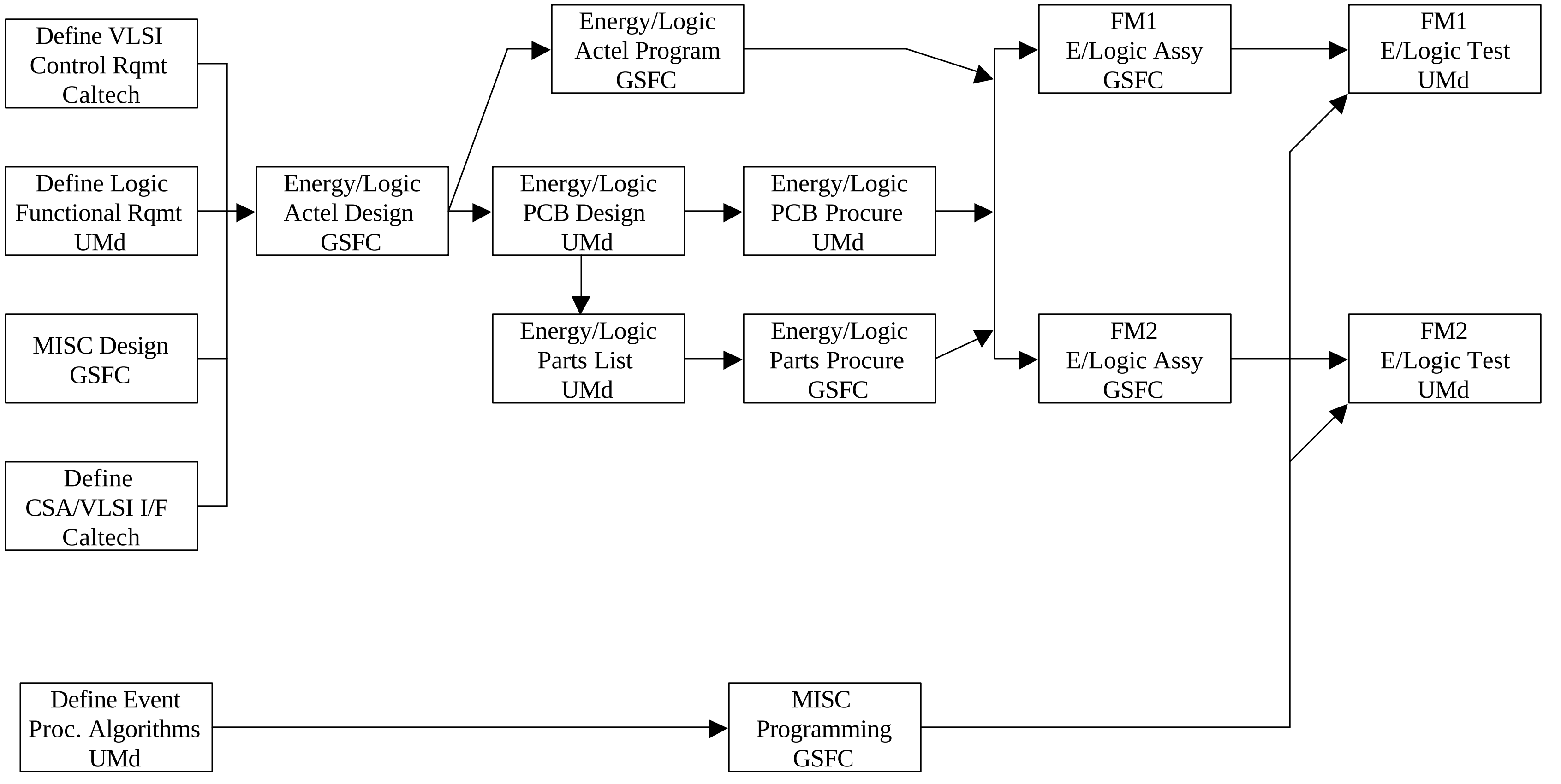
SIT Flow


FM1 Tel Deliver GSFC
FM1E/Logic Brd Deliver GSFC
FM1 TOF Deliver MPAe
FM1 HVPS Deliver UCB
FM1 MB Deliver GSFC
FM1 Housing Deliver GSFC
FM1 Tel Test UMd
FM1E/Logic Brd Test UMd
FM1 TOF Test MPAe
FM1 HVPS Test UMd
FM1 MB Test UMd
FM1 Assemble UMd
FM1 Debug UMd
FM1 Bench Test UMd
FM1Alpha Test UMd
FM1 Conf. Coat GSFC
FM1 ReAssemble UMd
FM1Funct. Test & Bench Cal UMd
FM2 Tel Deliver GSFC
FM2E/Logic Brd Deliver GSFC
FM2 TOF Deliver MPAe
FM2 HVPS Deliver UCB
FM2 MB Deliver GSFC
FM2 Housing Deliver GSFC
FM2 Tel Test UMd
FM2E/Logic Brd Test UMd
FM2 TOF Test MPAe
FM2 HVPS Test UMd
FM2 MB Test UMd
FM2 Assemble UMd
FM2 Debug UMd
FM2 Bench Test UMd
FM2Alpha Test UMd
FM2 Conf. Coat GSFC
FM2 ReAssemble UMd
FM2Funct. Test & Bench Cal UMd
Deliver to Caltech UMd

Telescope Flow



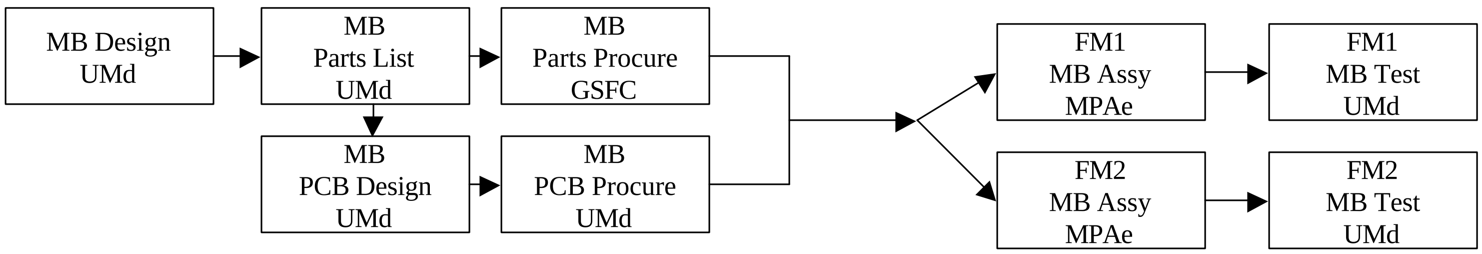
Energy/Logic Board Flow



TOF Flow

Prototype TOF Assy MPAe
Prototype TOF Test UMd
FM1 TOF Assy MPAe
FM1 TOF Test UMd
FM2 TOF Assy MPAe
FM2 TOF Test UMd

Motherboard Flow



GSE

- Electronics test setups
  - use at UMd only
  - board level tests
- CPU Simulator
  - SIT-level tests
  - use at UMd or whenever SIT needs to be tested alone
- Pulse Generator (1)
  - generates signals to stimulate TOF and energy circuits through test connector
  - battery powered
  - intended for use on S/C during SIT functional tests
- Mechanical GSE
  - carrying case (GSFC)

Current Status

- Telescope
  - Prototype built and tested
  - Sunshade/Cover and housing modifications for STEREO in progress
  - SSD, MCP, foil orders to be placed in Jan 02
- Energy/Logic
  - Preliminary VLSI specification received
  - Definition of I/F between CSA and VLSI in progress (Nov 1 01)
  - Definition of front-end logic in progress (Oct 15 01)
  - Definition of MISC algorithms has begun (no date)

Current Status (cont.)

- TOF
  - Prototype expected from MPAe Sept 17 01
  - GSE for testing prototype is underway and expected on time
- HVPS
  - Preliminary design exists
- Motherboard
  - waiting progress on other boards

WHO DOES WHAT
page 1 of 3

PROTOTYPE UNIT

	TASK	UMD	GSFC	CIT	UCB	MPAe
Prototype						
	Assemble Prototype Telescope		X			
	Test Prototype Telescope	X				
	Modify TOF Amp/Disc Design	X				
	Build/test prototype analog TOF board	X				
	Deliver Prototype Digital TOF system					X
	Integrate Analog and Digital TOF boards	X				
	Test Prototype TOF System	X				
	Charge Amp Design	X				
	Provide "Data Sheet" for VLSI			X		
	Assist Design to I/F CSA to VLSI			X		
	Outline SIT Logic Requirements	X				
	Detailed Front-end Logic Design		X			
	Prototype ACTEL Design		X			
	Specify CPU I/F requirements			X		
	Prototype MISC Design		X	X		
	Procure prototype MISC parts (ACTEL,RAM)		X	X		
	Generate data processing algorithms	X				
	Prototype MISC firmware		X			
	Design/Procure Prototype Energy PCB	X				
	Provide Prototype VLSI			X		
	Provide ACTEL Socket			X		
	Provide Other Proto E parts	X				
	Stuff Prototype Energy/Logic/MISC Board		X			
	Test Prototype Energy Board	X				
	Deliver prototype HVPS to UMD				X	
	Test Prototype HVPS	X				
	Test Harness design/build/test	X				
	Assemble/Test SIT Prototype	X				

WHO DOES WHAT
page 2 of 3

FLIGHT MODEL UNIT 1

	TASK	UMD	GSFC	CIT	UCB	MPAe
FM1						
	Procure SSD/MCP/Foils	X				
	Design/Build Sunshade/Cover		X			
	Build FM1 Telescope		X			
	Test FM1 Telescope	X				
	Generate TOF analog board parts list	X				
	Procure TOF analog board parts		X			
	Layout flight TOF analog board	X				
	Procure flight TOF analog board PCBs	X				
	Assemble FM1 TOF analog board		X			
	Test FM1 TOF analog board	X				
	Deliver FM1 TOF digital board					X
	Integrate FM1 TOF A and D boards	X				
	Test FM1 TOF	X				
	Procure flight Energy PCB	X				
	Generate final Energy board parts list	X				
	Deliver flight VLSI chips			X		
	Procure Parts: ACTELs, RAM			X		
	Other parts		X			
	Design flight front-end logic		X			
	Make flight front-end logic ACTEL		X			
	Generate final MISC firmware		X			
	Make flight MISC ACTEL		X			
	Assemble FM1 energy board		X			
	Test FM1 energy board	X				
	Deliver FM1 HVPS to UMD				X	
	Test FM1 HVPS	X				
	Layout and procure flight motherboard PCB	X				
	Procure parts for motherboard		X			
	Assemble FM1 motherboard		X			
	Test FM1 motherboard	X				
	Assemble and Test FM1 unit	X				
	Conformal coat E, Logic and MB		X			
	Post-coat assy & test	X				

WHO DOES WHAT page 3 of 3

FLIGHT MODEL UNIT 2

	TASK	UMD	GSFC	CIT	UCB	MPAe
FM2						
	Build FM2 Telescope		X			
	Test FM2 Telescope	X				
	Assemble FM2 TOF analog board		X			
	Test FM2 TOF analog board	X				
	Deliver FM2 TOF digital board					X
	Integrate FM2 TOF A and D boards	X				
	Test FM2 TOF	X				
	Assemble FM2 energy board		X			
	Test FM2 energy board	X				
	Deliver FM2 HVPS to UMD				X	
	Test FM2 HVPS	X				
	Assemble FM2 motherboard		X			
	Test FM2 motherboard	X				
	Assemble and Test FM2 unit	X				
	Conformal coat E, Logic and MB		X			
	Post-coat assy & test	X				
	Deliver FM1 and FM2 to Caltech	X				
GSE						
	CPU Simulator	X				
	SIT Stimulus Unit	X				

SIT Verification Matrix

			Verification Matrix for STEREO/IMPACT/SEP/SIT																			Revision Date: 7/20/01
																						Revision Number: 1
Hardware Description		Tests																				
Level of Assembly	Item	Vacuum	Alphas	Elect. test, rm. Temp	Bench Calibration	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Shock	Acoustics	Thermal Vacuum	Voltage margins	Thermal cycle	Thermal balance	Life Test	EMC/EMI	Magnetics	Beam Calibration	Bakeout	Contamination	Comments
C	Detectors, F		X									X										
C	Foils PT										X											
C	Telescope PF,F	X	X																		X	
C	Energy board, EM			X		X	X						X									
C	Energy board, F			X																	X	
C	TOF Board, EM			X		X	X						X									
C	TOF Board, F			X																	X	
C	HVPS EM			X		X	X						X									
C	HVPS F			X																	X	
I	Instrument W/O Telescope																			*2		
I	Instrument, PF	X	X	X	X	X	X	X	X	*1		X	X	X	X	X	X	X	X		X	Performed at SEP level or higher
I	Instrument, F	X	X	X	X	X	X	X	X	*1		X	X	X	X	X	X	X	X		X	Performed at SEP level or higher

Legend:

Level of Assembly	Unit Type		X =	Test required
			A =	Analysis
C = Component	BB	Breadboard		
I = Instrument	EM	Engineering Model	*1	Sine burst test during vibration testing
	PT	Prototype	*2	As required
	PF	Protoflight		
	F =	Flight		

Parts Lists - Energy/Logic

CSA FET - 2N6550
CSA Hybrid - Amptek A250
Resistors - RNC-50, -55, -60
Capacitors - CKR06, CDR01, CDR05,CDR06

Connectors - Nanohex, Nanonics

Caltech VLSI

Clock - TBD
ACTEL - TBD
RAM - TBD

DAC-08 - open to suggestions on more modern part
LM108 - open to suggestions on more modern part

Parts Lists - Analog TOF

	Type:	Part No:	Package:	Manufacturer	Description	Electronics Fu	Distributor:	Additional Info:	Qualification:
SMD Resistors:									
	8R2	M55342K06B8D2R	0805	Kemet	Chip Resistor				MIL
	30R	M55342K06B30D0R	0805	Kemet	Chip Resistor				MIL
	51R1	M55342K06B51D1R	0805	Kemet	Chip Resistor				MIL
	56R	M55342K06B56D0R	0805	Kemet	Chip Resistor				MIL
	75R	M55342K06B75D0R	0805	Kemet	Chip Resistor				MIL
	100R	M55342K06B100D0R	0805	Kemet	Chip Resistor				MIL
	150R	M55342K06B150D0R	0805	Kemet	Chip Resistor				MIL
	360R	M55342K06B360D0R	0805	Kemet	Chip Resistor				MIL
	510R	M55342K06B510D0R	0805	Kemet	Chip Resistor				MIL
	750R	M55342K06B750D0R	0805	Kemet	Chip Resistor				MIL
	1K5	M55342K06B1E50R	0805	Kemet	Chip Resistor				MIL
	1K5	M55342K06B1E80R	0805	Kemet	Chip Resistor				MIL
	1K5	M55342K06B2E00R	0805	Kemet	Chip Resistor				MIL
	5K1	M55342K06B5E10R	0805	Kemet	Chip Resistor				MIL
	6K98	M55342K06B6E98R	0805	Kemet	Chip Resistor				MIL
	7K5	M55342K06B7E50R	0805	Kemet	Chip Resistor				MIL
	10K	M55342K06B10E0R	0805	Kemet	Chip Resistor				MIL
	100K	M55342K06B100ER	0805	Kemet	Chip Resistor				MIL
SMD Capacitors									
	15pF	CDR01BP150BJWS	CDR01	Kemet	Ceramic Chip Capacitor				MIL
	470pF	CDR01BP471BJWS	CDR01	Kemet	Ceramic Chip Capacitor				MIL
	1000pF	CDR01BX102BKWS	CDR01	Kemet	Ceramic Chip Capacitor				MIL
	10nF	CDR31BX103AKWS	CDR31	Kemet	Ceramic Chip Capacitor				MIL
	12nF	CDR31BX123AKWS	CDR31	Kemet	Ceramic Chip Capacitor				MIL
Solid Tantalum SMD:									
	1.5uF/15V CWR	CWR11HH155KB-X	CWR11A	Kemet	Solid Tantalum C	Power Blocking	TTI	J=+-5% Tol., Fail:C=0.01	MIL_C-55365/8
Active Parts:									
	AT41435	AT41435	MicroX	Agilent Techn	RF Transistor				commercial / ceramic package
	MP4T636535	MP4T636535	MicroX	MPulse	RF Transistor			alternative to Agilent	JANTX available
	SPT9687SIN		PDIP	SPT	UHS Comparator				commercial / plastic package (
	SPT9687SIC		CLCC	SPT	UHS Comparator				commercial / ceramic LCC pac
	AD96687TQ/883		CDIP	Analog Devic	UHS Comparator			obsolete / some old	military but old parts!
Semiconductors:									
	1N5711 US J	1N5711 US JANTX	Amelf	Microsemi	Shottky Diode		Protec GmbH		Military
Inductors:									
	15uH M0820-	15uH M0820-52K	M0820	Delevan	Surface Mount Inductor		Ing Büro Grosshening		Military M83446/21
Connectors:									
	SMA			Radiall	Connector				
	DUALLOBE			Nanonics Dua	Connector				

Parts Lists - Digital TOF

TBS

Parts Lists - HVPS

Item	Quantity	Reference	Part	Part Number
1	6	C1,C2,C15,C16,C22,C23	2200pF, 20%, 7500V	7030B222K752SMC
2	2	C10,C3	10uF, 10%,35V	M39003/10-2544S
3	2	C9,C4	.1uF, 10%, 50V	M39014/1-1593
4	14	C17,C18,C20,C21,C24,C26, C29,C30	2200pF, 10%, 2000V	2020B222M302S
5	1	C6	36pF, 1%, 200V	CCR05CG360FS
6	3	C7,C25,C31	.01uF, 10%, 100V	M39014/1-1575
7	1	C19	1000pF, 1%, 200V	CCR05CG102FS
8	1	C27	3.9uF, 10%, 75V	MIL-C-39003/10-2114S
9	1	C28	.1uF, 10%, 100V	M123A02BXC104KC
10	14	D1,D2,D3,D4,D5,D7,D9,D10, D12,D14,D15,D16,D17,D18	JANTX1N6515U	JANTX1N6515U
11	2	D13,D6	JTXV1N5711	JTXV1N5711
12	4	D8,D11,D19,D20	1N4938	JANTXV1N4938
13	2	FB2,FB1	FERRITE BEAD	TUB3.5/1.3/3.3/3E2A
14	6	J1,J2,J3,J4,J5,J7	Reynolds 167-3771	Reynoldsn167-3771
15	1	J6	M83513/04-A11N	M83513/04-A11N
16	1	L1	Common Mode 3	Custom SSL
17	2	Q3,Q1	3N170	3N170
18	2	Q4,Q2	2N3700	JANTXV2N3700
19	1	R1	1.43 Meg, 1%, .125W	D55342H07B1F00R
20	1	R2	1000 MEG, 1%	MOX 1125-23 1000 MEG 1%
21	6	R3,R4,R13,R14,R21,R22	1M 1%, .25W	RLR-07C1004FS
22	3	R5,R15,R23	100K, 1%, .25W	RLR-07C1003FS
23	4	R6,R11,R17,R20	100K, 1%, .125W	D55342H07B100ER
24	1	R7	1.00K, 1%, .125W	D55342H07B1E00R
25	1	R8	1.00K, 1%, .25W	RLR-07C1001FS
26	1	R9	10M	TBD
27	2	R31,R10	49.9K, 1%, .25W	D55342K07B49E9R
28	1	R12	2.5M	TBD
29	2	R16,R19	TBD	
30	1	R18	20 Ohms, 1%, .125W	D55342H07B20D0R
31	2	R24,R27	562, 1%, .125W	D55342H07B562DR
32	1	R25	15.0K, 1%, .125W	D55342H07B15E0R
33	1	R26	51.1K, 1%, .125W	D55342H07B51E1R

Materials Lists

Hazards

- Thin foil subject to breakage if touched
  - behind acoustic cover, open only in thermal vacuum test
- Detectors subject to contamination from chemicals and humidity
  - continuous purge with dry GN2
  - limit exposure
- High voltage (4kv)
  - current limited to 10s of uA
  - inside telescope and HVPS only, not exposed
  - turned on only during thermal vacuum test
  - low voltage mode (few hundred volts) for other testing, still not exposed
- Radioactive Source
  - used during thermal vacuum only, Am241, 10s of uCi

SIT Performance Requirements

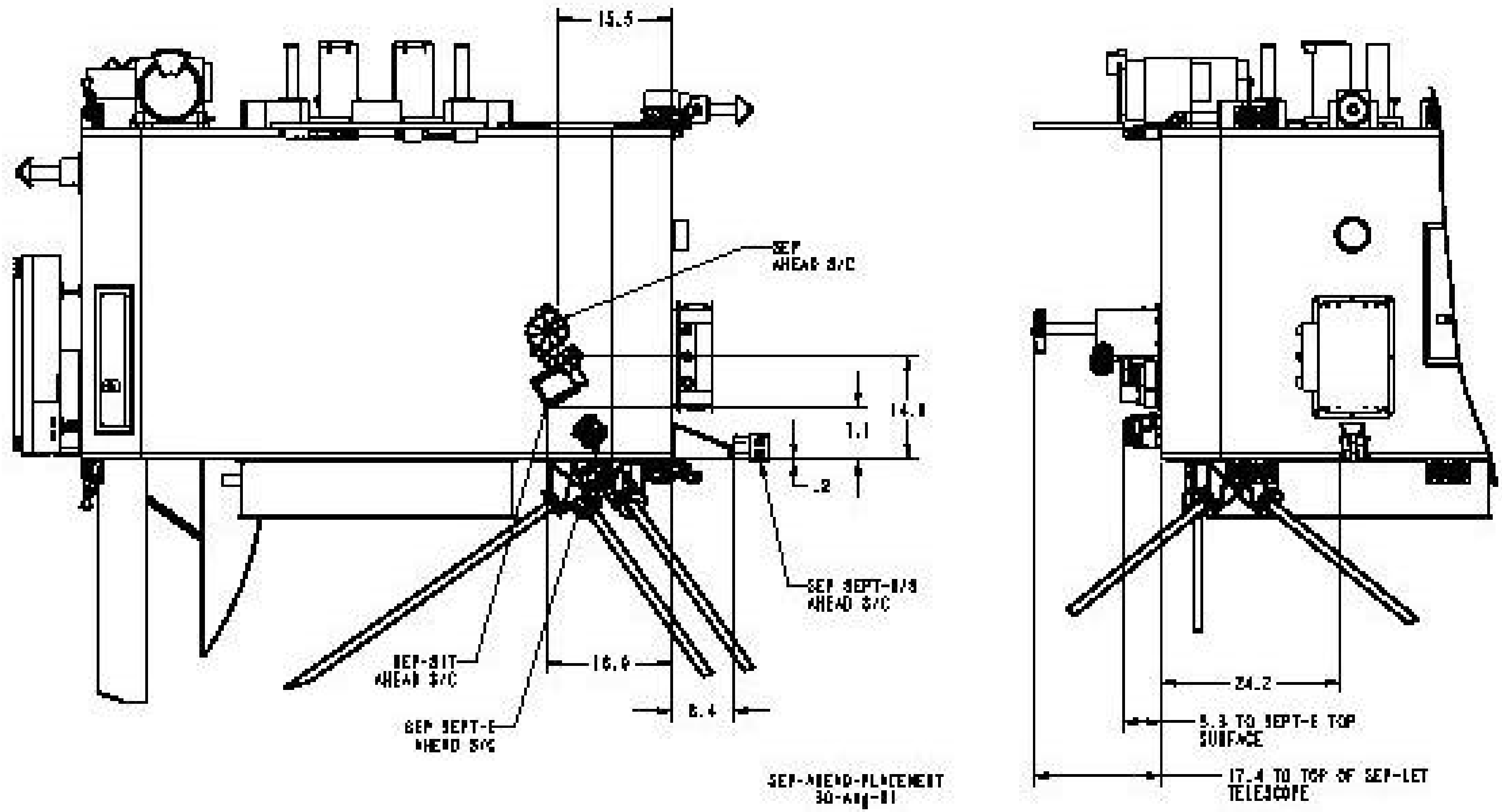
Description	Goal	Requirement	Current
FOV	17 x 44 degrees	17 x 44 degrees	17 x 44 degrees
Energy	30-2000 keV/nuc, He-Fe	30-2000 keV/nuc, He-Fe	not yet tested
Mass Resolution	0.85 AMU (^{16}O at 100keV/nuc)	0.85 AMU (^{4}He at 1MeV/nuc)	not yet tested
Energy Resolution	20 keV FWHM	35keV FWHM @22C	not yet tested
Geometric Factor	0.4cm^2 ster	0.4cm^2 ster	0.4cm^2 ster
Background	10^{-2} events/sec in quiet time	10^{-2} events/sec during vac test	not yet tested
Max Event rate	1000 events/sec	1000 events/sec	not yet tested
Time Resolution	1 minute	15 minutes	1-5 minutes

SEP Mechanical Design/ Fields of View

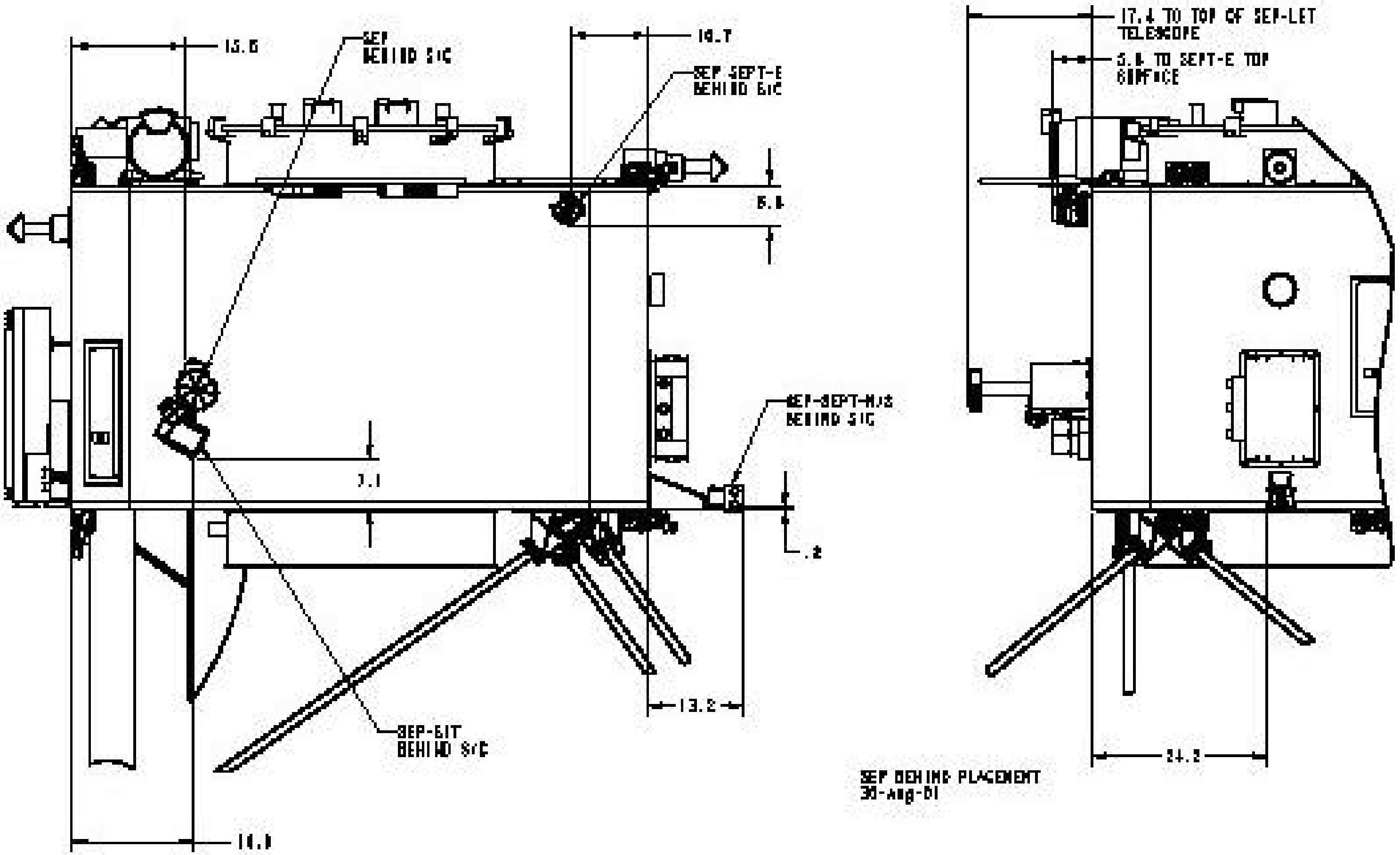
Sandy Shuman, GSFC

Tycho von Rosenvinge, GSFC

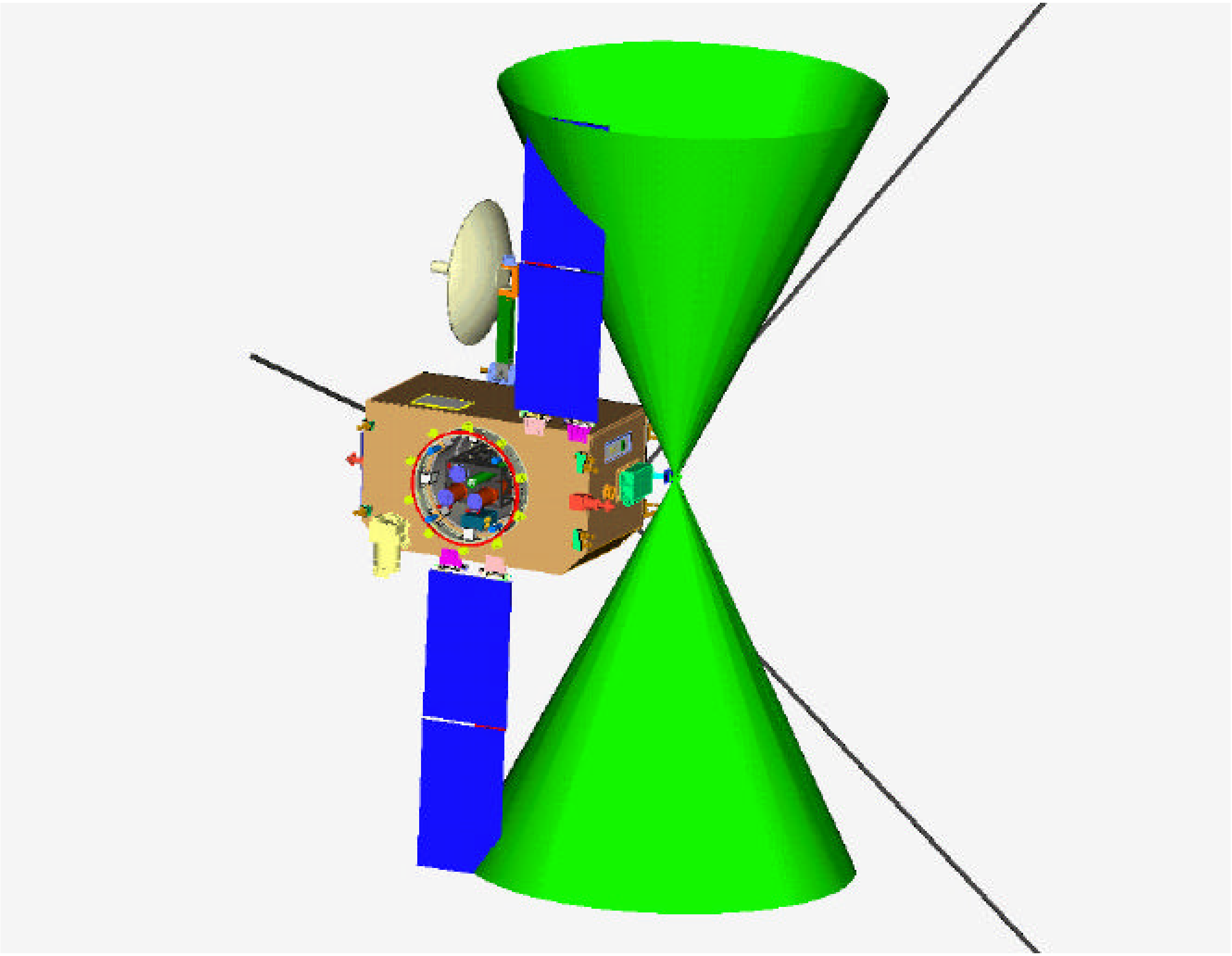
SEP Locations on the Ahead Spacecraft



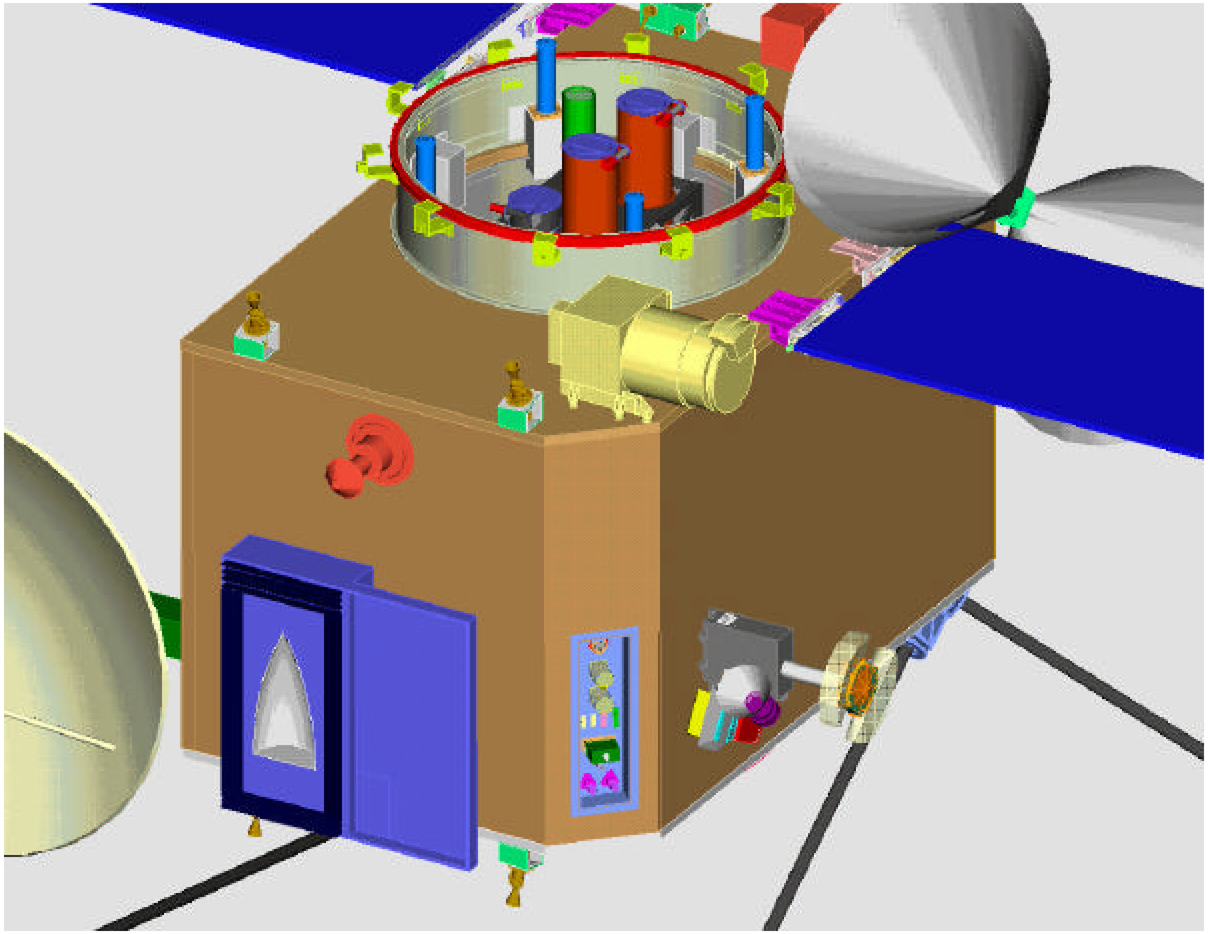
SEP Locations on the Behind Spacecraft



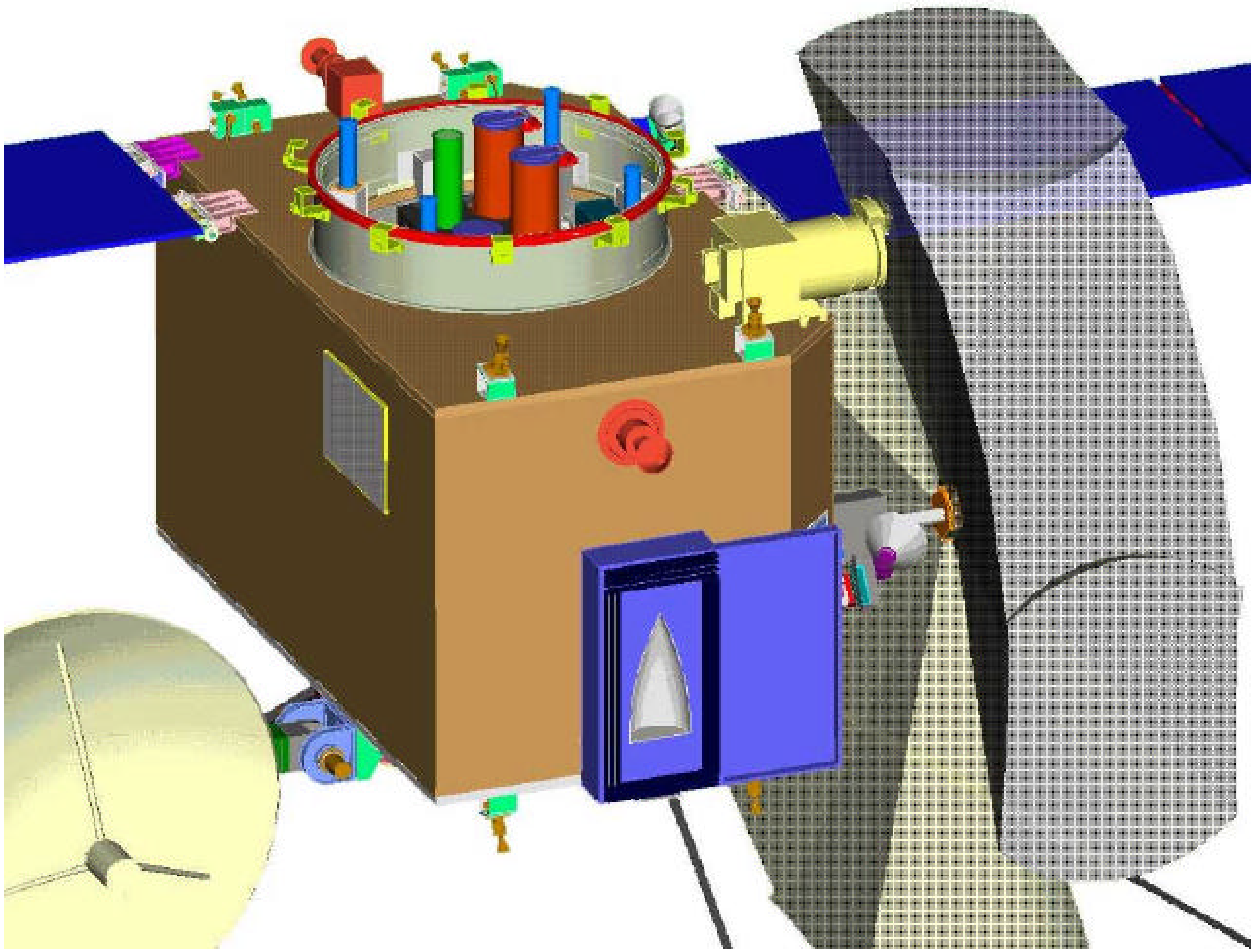
SEPT North-South Fields of View



LET FOV Impingement with Solar Array on Behind Spacecraft



LET Field of View Impingement with PLASTIC … Much Reduced!



Mass Allocation

SEP resources: Mass [g]

Component	**PDR**	**Peer Rev.**	
SIT sensor & door	500	500	
SIT elec. boards & wiring	370	370	
SIT HVPS	160	160	
SIT encl. & hdwr	200	200	
------------------------	------	------	
SIT subtotal:	**1230**	**1230**	
SEPT-NS	520	520	w/o harness
SEPT-E	520	540	w/ 10cm har
------------------------	------	------	
SEPT subtotal:	**1040**	**1060**	
LET det. & housing	515	515	
LET electronics	235	235	
LET subtotal:	**750**	**750**	

MASS Allocation … Cont

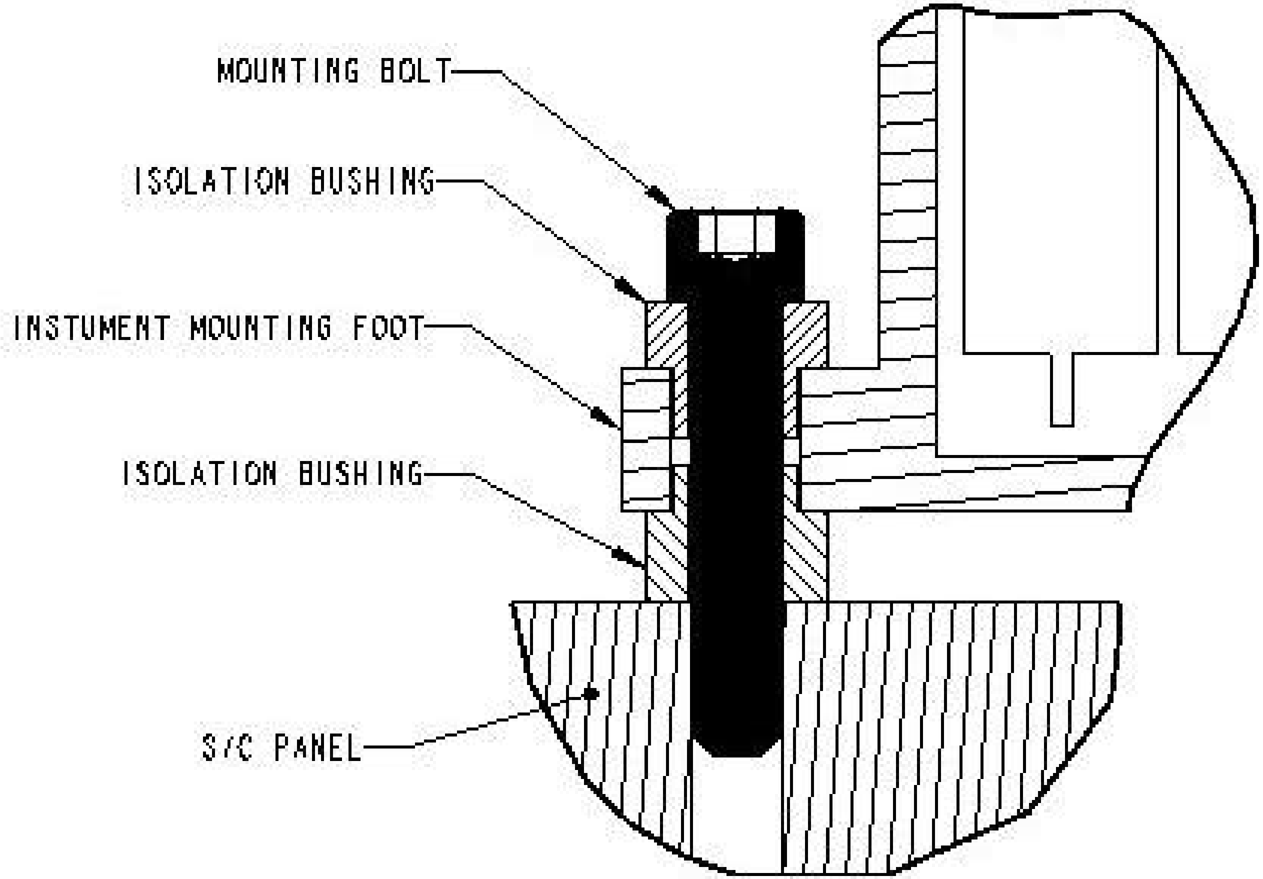
Component	PDR	Peer Rev.
HET det. & housing	500	460
HET electronics	160	160
-----------------------	------	------
HET subtotal:	**660**	**620**
Cent. elec. encl. & hdwr	1500	1030
El. boards, shields, harness	1090	1090
-----------------------	------	------
Central electr. subtotal:	**2590**	**2120**
SEPT-NS bracket	270	270
LET bracket	600	600
SEP bracket	N/A	N/A
-----------------------	------	------
SEP subtotal:	**7140**	**6650**

MASS Allocation … Cont

Component	PDR	Peer Rev.
SEPT-NS Ahead harness (1.7 m)	185	150
SEPT-NS Behind harness (2.9 m	293	150
SEPT-E Ahead harness (0.4 m)	73	N/A
SEPT-E Behind harness (2.3 m)	240	N/A
Thermal blankets	120	100
SEP Ahead Total	7518	6900
SEP Behind Total	7793	6900

Note: The increased harness weights are to be covered by the Project as part of the solution to SEP field-of-view problems associated with the new spacecraft configuration. This still leaves an overall weight growth of 510 g (7.4%)

Typical Mounting Foot Showing Thermal Isolation



IMPACT/SEP Thermal Design

John Hawk, GSFC
Sandy Shuman, GSFC
Tycho von Rosenvinge, GSFC

STEREO Thermal Environment

Early Orbit: Up to 40 minute coast at 100 nautical miles altitude; non-spinning spacecraft?

Ahead Spacecraft: Maneuvers for up to first 60 days can off-point from sun-pointing by up to 45 degrees for up to 40 minutes (single lunar swing-by

Behind Spacecraft: Maneuvers for up to first 90 days can off-point from sun-pointing by up to 45 degrees for up to 40 minutes (two lunar swing-bys)

Extreme mission orbit conditions:

Ahead S/C: Perihelion = 0.879 AU, Aphelion = 1.040 AU

Behind S/C: Perihelion = 0.960 AU, Aphelion = 1.131 AU

Nominal orbit:

Ahead S/C: Perihelion = 0.943 AU, Aphelion = 0.979 AU

Behind S/C: Perihelion = 1.003 AU, Aphelion = 1.083 AU

SEP Temperature Limits (^{O} C)

Component	Preferred Operating	In-Spec Operating	Non-Operating
HET			
Detectors	-15 to +10	-25 to +35	-25 to +40
Electronics	-15 to +10	-25 to +40	-25 to +50
LET			
Detectors	-15 to +10	-25 to +35	-25 to +40
Electronics	-15 to +10	-25 to +40	-25 to +50
SIT			
Detectors	-15 to +10	-25 to +30	-25 to +35
Electronics	-15 to +10	-25 to +40	-25 to +50
SEPT			
Detectors	-15 to +10	-25 to +35	-25 to +50
Electronics	-15 to +10	-25 to +40	-25 to +50

Thermal Blankets

- Designs to be supplied by GSFC to APL
- Blankets to be fabricated by APL; 18-layer typical unless tight bends (~ 600 g/m^2)
- Typical Uses:

  -Ag Teflon blanket with ITO coat for most surfaces in sunlight (somewhat fragile, but SECCHI is using it)

  -Black Kapton blanket with Ge coat for surfaces not directly in sunlight

Can also use ITO coated silver conductive composite deposited on the aluminum or on Kapton which is then bonded to the aluminum

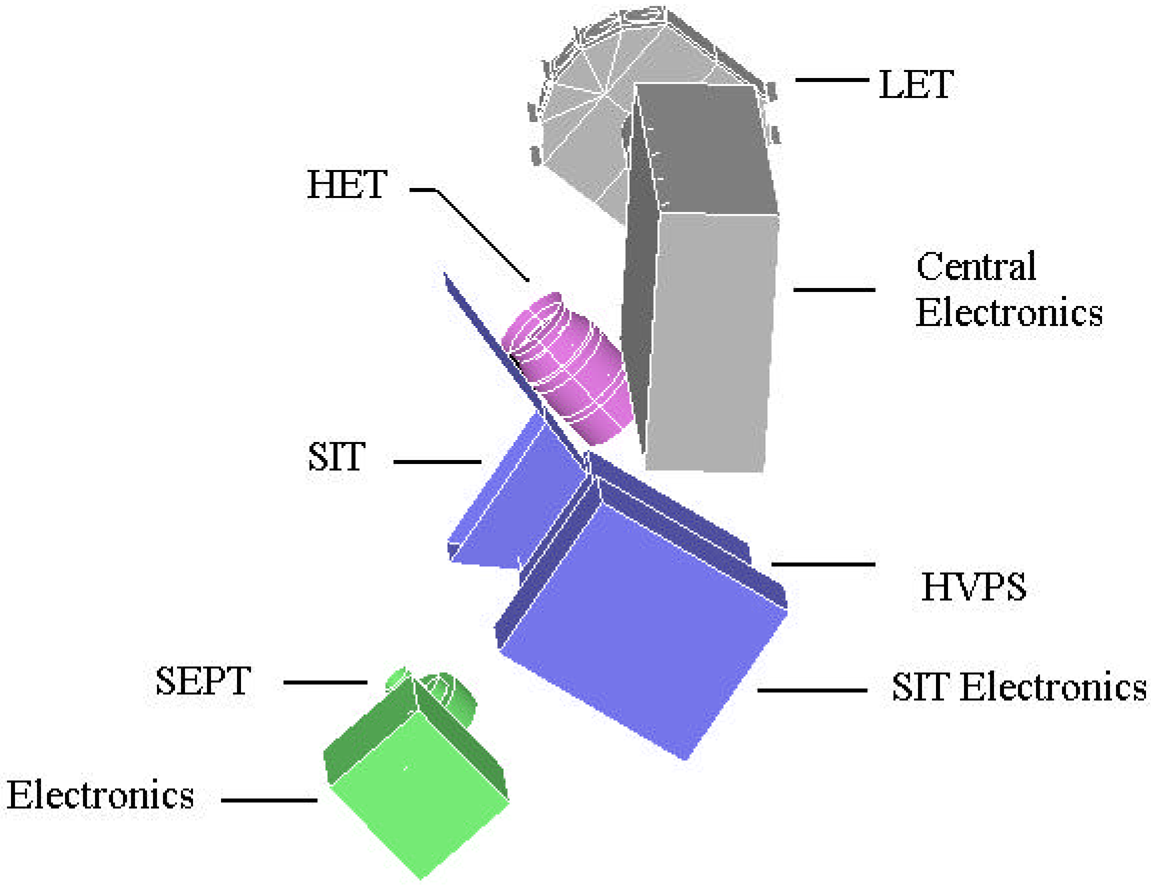
Modeling Assumptions

- Spacecraft panel interface temperature range of -23C to +55C
- SEP and SEPT are thermally isolated on Ultem brackets
- SEP and SEPT are thermal blanketed at spacecraft interface
- 10” x 10” area, plus 12.5% of spacecraft panel used as radiator

Weight/Power Dissipation in Each SEP Subsystem

Component	Power Dissipation (W)	Mass (g)
SIT	1.126	1070
HVPS	0.16	160
SEPT	1.04	1330
LET	0.435	1350
HET	0.25	620
Cent. Elec	1.51	2120
TOTAL	**4.521**	**6650**

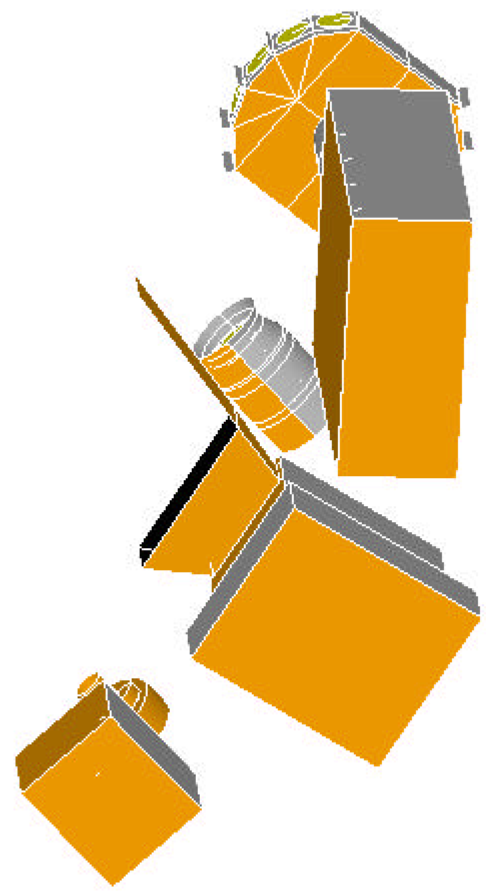
Sample Thermal Model



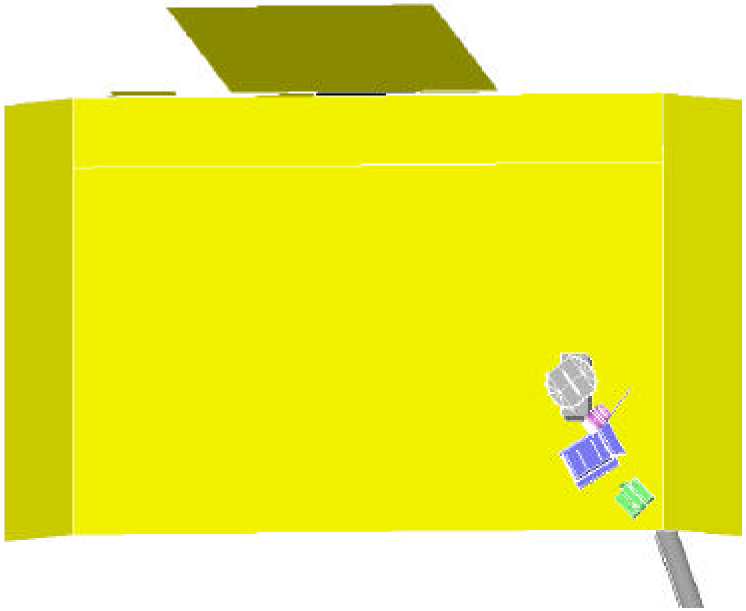
Sample Thermal Model With MLI

MLI

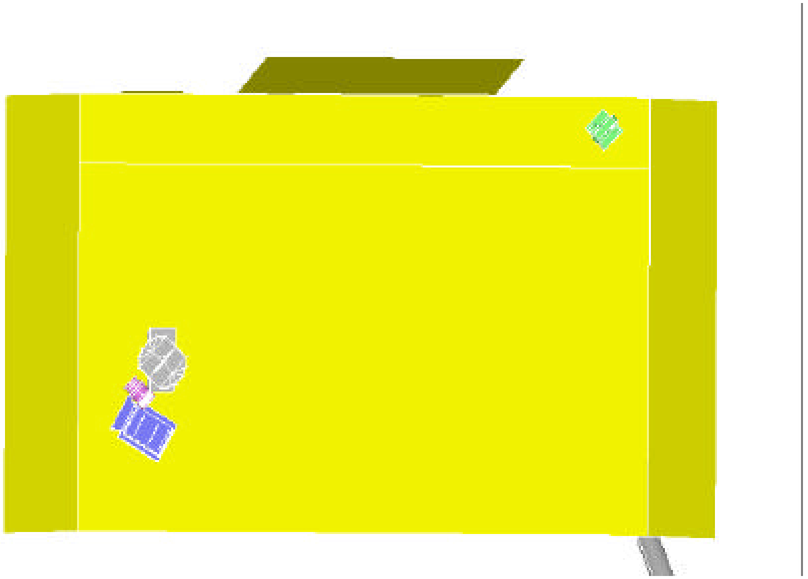
ITO Silver Conductive
Composite Coating
$\alpha = 0.20$ $\varepsilon = 0.66$



Ahead And Behind Thermal Models



Ahead



Behind

Currently Modeling

Thermal models are now built and ready to develop the SEP thermal design

- Nominal, Hot, and Cold Cases:
  - Ahead S/C: Perihelion = 0.879 AU, Aphelion = 1.040 AU
  - Behind S/C: Perihelion = 0.96 AU, Aphelion = 1.131 AU
  - Model pointing directly at sun and off-pointing by 5 degrees for each of the above
- Transient Analysis
  - Off-Pointing from Sun 45 Degrees for 40 minutes
- Adjusting MLI Blanket and coating locations to meet operating temperatures
- Early Orbit

Thermal Concerns

- Need to determine what survival heaters are needed. Is this power available?
- Need to determine whether operational heaters are needed. Is this power available?
- SEPT magnet geometry not yet included in SEPT model
- SEP can be completely shaded during 45 degree off-pointing

SEP Integration and Test

Tycho von Rosenvinge, GSFC

SEP I&T

- **Four instruments tested separately to the extent possible**
  - **LET at Caltech/JPL**
  - **HET at GSFC**
  - **SIT at UMd/GSFC**
  - **SEPT at Kiel**
- **SEP Common integrated & tested at Caltech**
  - **Low Voltage Power Supply from UCB**
  - **Detector bias supply from Space Instruments**
  - **Analog/post-reg board from Space Instruments**
  - **Logic board from Caltech**
  - **Mechanical parts from GSFC**
  - **Telescopes**
- **SEP Common/IDPU interface test at UCB and/or Caltech**
- **Integrate into SEP system at Caltech**
- **Test SEP at Caltech**
- **EMI/EMC at UCB**

SEP/SEPT Verification Matrix

				Verification Matrix for STEREO/IMPACT/SEP Instruments																		Revision Number ____________
																						Revision Date
Hardware Description				Tests																		
Level of Assembly	Item	Spacecraft	Quantity	Thermal Analysis	Struct. Analysis	Modal Survey/ Sine Sweep	Loads Test/ Sine Burst	Random Vibration	Mechanical Shock	Acoustics	Mass Properties	Pressure Profile	Mechanical Function	Life Test	EMC/EMI	Magnetics	Leak	Thermal	Thermal Balance	Thermal Vacuum	Bakeout	Comments
I	SEPT-E (T)		1	A	A					X			X	X	X	X		X				Engineering Model
I	SEPT-E (PF)	A	1			X		X		X	X		X	X	X	X			X	X		Test to qualification level
I	SEPT-E (F2)	B	1			X		X		X	X		X	X	X				X	X		Test to acceptance level
I	SEPT-NS (F1)	A	1			X		X		X	X		X	X	X				X	X		Test to acceptance level
I	SEPT-NS (F2)	B	1			X		X		X	X		X	X	X				X	X		Test to acceptance level

LEGEND:

Level of Assembly	Unit Type	X - Test Required
		T - Test if Analysis Indicates
I = Instrument	PT = Prototype	A - Analysis
C = Component	PF = Protoflight	
L = Laboratory	F = Flight	
	S = Spare	

SEP/SIT Verification Matrix

Verification Matrix for STEREO/IMPACT/SEP/SIT

Revision Date: 7/20/01
Revision Number: 1

Hardware Description		Tests																				
Level of Assembly	Item	Vacuum	Alphas	Elect. test, rm. Temp	Bench Calibration	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Shock	Acoustics	Thermal Vacuum	Voltage margins	Thermal cycle	Thermal balance	Life Test	EMC/EMI	Magnetics	Beam Calibration	Bakeout	Contamination	Comments
C	Detectors, F		X									X										
C	Foils PT										X											
C	Telescope PF,F	X	X																		X	
C	Energy board, EM			X		X	X						X									
C	Energy board, F			X																	X	
C	TOF Board, EM			X		X	X						X									
C	TOF Board, F			X																	X	
C	HVPS EM			X		X	X						X									
C	HVPS F			X																	X	
I	Instrument W/O Telescope																			*2		
I	Instrument, PF	X	X	X	X	X	X	X	X	*1		X	X	X	X	X	X	X	X		X	Performed at SEP level or higher
I	Instrument, F	X	X	X	X	X	X	X	X	*1		X	X	X	X	X	X	X	X		X	Performed at SEP level or higher

Legend:

Level of Assembly	Unit Type			
			X =	Test required
			A =	Analysis
C = Component	BB	Breadboard		
I = Instrument	EM	Engineering Model	*1	Sine burst test during vibration testing
	PT	Prototype	*2	As required
	PF	Protoflight		
	F =	Flight		

SEP/LET Verification Matrix

Verification Matrix for STEREO/IMPACT/SEP/LET

Revision Date: 7/19/01

Revision Number: 1

Hardware Description		Tests																				
Level of Assembly	Item	Noise & Brkdown	Thermal vacuum	Alphas	Elect. test, rm. Temp	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Shock	Acoustics	Pressure change	Voltage margins	Thermal cycle	Thermal balance	Life Test	EMC/EMI	Magnetics	Leak	Bakeout	Contamination	Comments
C	Detectors, PT & F	X	X	X	X	X	X		X					X								
C	VLSI, PF				X	X	X															
C	Hybrids, PT & F				X	X	X												X		X	
C	LET detector board, EM				X	X	X															
C	LET detector board, F				X																X	
C	LET MISC board, EM				X	X	X						X									
C	LET MISC board, F				X																X	
C	Connectors, F															X					X	
I	Instrument, EM				X	X	X						X	X								
I	Instrument, F		X	X	X	X	X	X	X	A	X	A	X		X	X	X			X	X	

Legend:

Level of Assembly	Unit Type			
			X =	Test required
			A =	Analysis
C = Component	BB =	Breadboard		
I = Instrument	EM =	Engineering Model		
	PT =	Prototype		
	PF =	Protoflight		
	F =	Flight		

SEP/HET Verification Matrix

Verification Matrix for STEREO/IMPACT/SEP/HET

Revision Date: 7/19/01
Revision Number: 1

Hardware Description		Tests																			
Level of Assembly	Item	Noise & Brkdown	Thermal vacuum	Alphas	Elect. test, rm. Temp	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Shock	Acoustics	Pressure change	Voltage margins	Thermal cycle	Thermal balance	Life Test	EMC/EMI	Magnetics	Leak	Bakeout	Contamination	Comments
C	Detectors, PT & F	X	X	X	X	X	X		X					X								
C	VLSI, PF				X	X	X															
C	Hybrids, PT & F				X	X	X												X		X	
C	HET board, EM				X	X	X						X									
C	HET board, F				X																X	
C	Connectors, F															X					X	
I	Instrument, EM				X	X	X						X	X								
I	Instrument, F		X		X	X	X	X	X	A	X	A	X		X	X	X			X	X	

Legend:

Level of Assembly	Unit Type			
			X =	Test required
			A =	Analysis
C = Component	BB =	Breadboard		
I = Instrument	EM =	Engineering Model		
	PT =	Prototype		
	PF =	Protoflight		
	F =	Flight		

SEP Common Electronics Verification Matrix

Verification Matrix for STEREO/IMPACT/SEP/SEP Common

Revision Date: 7/19/01
Revision Number: 1

Hardware Description		Tests																				
Level of Assembly	Item	Noise & Brkdown	Thermal vacuum	Alphas	Elect. test, rm. Temp	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Shock	Acoustics	Pressure change	Voltage margins	Thermal cycle	Thermal balance	Life Test	EMC/EMI	Magnetics	Leak	Bakeout	Contamination	Comments
C	LVPS, EM				X	X	X						X				X					
C	LVPS, F				X																X	
C	Analog Post-reg, EM				X	X	X						X									
C	Analog Post-reg, F				X																X	
C	Detector bias supply, EM				X	X	X						X				X					
C	Detector bias supply, F				X																X	
C	Logic board, EM				X	X	X						X									
C	Logic board, F				X									X							X	
C	Connectors, F															X					X	
C	Harnesses, F																				X	
I	Instrument, EM				X	X	X						X				X					
I	Instrument, F		X		X	X	X	X	X	A	X	A	X		X	X	X			X	X	

Legend:

Level of Assembly	Unit Type			
C = Component	BB =	Breadboard	X =	Test required
I = Instrument	EM =	Engineering Model	A =	Analysis
	PT =	Prototype		
	PF =	Protoflight		
	F =	Flight		

SEP Issues and Concerns

Tycho von Rosenvinge, GSFC

SEP Issues and Concerns

- LET L1 Detector Development
- Vibration (SEPT-N/S, LET)
- VLSI schedule
- Potential interference between SEPT-E field-of-view on the Behind Spacecraft and separation ring clamp
- LET Detectors/ Thermal
- Survival heaters (none yet budgeted, pending outcome of thermal analysis)
- ITAR
- Definition of early orbit activities/pointing
- Hydrazine plumes?
- SIT Time-of-Flight
- Compliance with contamination control requirements
- Lack of travel budget for extra reviews and end-to-end tests
- Funding profile
- Staffing is lean

International Activities, SEP

- TOF system being built by Max/Planck Lindau using UMd designs
  - GSFC arranged for drawings & documents to be transferred
- Caltech/U. Kiel/EsTEC
  - Regular teleconferences seem to be adequate to this point
- Caltech/Micron/LBL/JPL interaction on L1 detector
  - Micron Ltd. will process front side of 300 um thick, 4” wafers
  - Wafers will be sent to LBL/JPL for thinning to 20 um in detector active areas
  - Wafers will be returned to Micron for processing the backside
  - We’ve discussed this with Caltech/JPL counsel; waiting for advice
- May need GSFC assistance with other hardware transfers
  - No TAA’s likely at Caltech
  - SEPT hardware needs to be imported and possibly exported

Action Item Status from SEP/MAG Peer Review (1 of 2)

Item	Action	Status	Status
159	SEP Software Configuration Control	Plan Documented in SEP Software Development Plan	In Review by GSFC
160	Parts Radiation tolerance, especially Actel	Radiation effects are considered in parts selection	Closed
161	Need a Requirements Matrix	Matrix due at PDR	Open
163	MISC test plan	Complete	Closed
164	New Actel Availability backup plan	Given STEREO schedule slip, this is no longer considered a significant risk	Closed
165	Fixed length telemetry packet impact	Preliminary packet formats have been developed	Closed
166	6” Mag sensor separation from boom harness requirement	Incorporated into boom design	Closed
167	IMPACT Schedule	Both top level milestone and detailed subsystem schedules exist for almost all subsystems	Open
168	SEPT Cover Design	Cover selected, detailed design in progress	Closed
169	SEPT Purge requirements	Provided	Closeable

Action Item Status from SEP/MAG Peer Review (2 of 2)

Item	Action	Status	Status
170	Select SIT detector type	Done (surface barrier)	Closed
171	Identify SIT HV Contamination Control Requirements	Bakeout per contamination control plan	Closed
172	LET mast surface treatment	Per materials list, due at PDR	Open
173	Materials List	Per materials list, due at PDR	Open
175	Materials List	Per materials list, due at PDR	Open
176	Contamination Control Plan	In Work	Open
177	Contamination Sensitivity	In Work	Open
178	APL Magnetics Lead	MAG CoI to have periodic MAG workshops at APL	Closeable
179	SIT HVPS Frequency Waiver	Informally closed, not yet formally presented	Open
180	SIT TOF Power Increase	Included in baseline	Closed
181	EMC Plan Should Require checking at MAG frequencies	MAG Requests only a paper survey at this time	Open
182	Mag Heater Frequency Control	Crystal-synchronized	Closeable

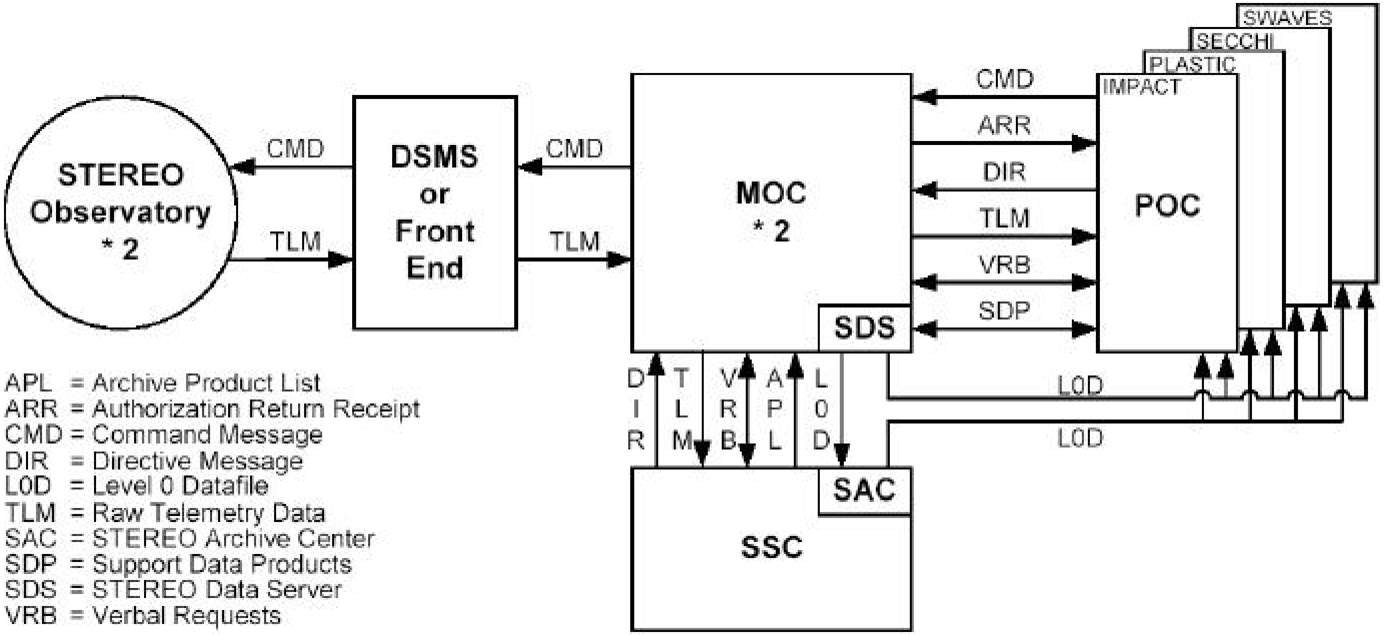
Mission Operations and Data Analysis

IMPACT Mission Operations Facilities

- **The IMPACT team shall use the EGSE as the basis of the IMPACT POC for commanding and real time telemetry**
  - The same EGSE that was used throughout Instrument and Observatory testing
  - Command scripting capability allows for semi-automated operations
  - Automated state of health monitoring warns of any out-of-limit conditions
  - The EGSE shall be directly connected to the MOC via TCP/IP sockets as described in the MOC/POC ICD.
  - The EGSE shall be co-located with the MOC during Commissioning phases, and shall be left there in case needed for any later real-time diagnostics
  - A remote copy of this EGSE at UCB shall be used for submitting commands during normal operations.

- **A suite of data reduction and analysis software shall be added to the POC to perform the offline data processing.**
  - This software shall run on distributed systems, using data FTPed from the STEREO MOC as described in the MOC/POC ICD.
  - UCLA shall provide web-accessible Summary Data Product

MOC / POC Interface



APL = Archive Product List
ARR = Authorization Return Receipt
CMD = Command Message
DIR = Directive Message
L0D = Level 0 Datafile
TLM = Raw Telemetry Data
SAC = STEREO Archive Center
SDP = Support Data Products
SDS = STEREO Data Server
VRB = Verbal Requests

Commissioning

- During Commissioning, and any other Real Time operations, IMPACT personnel shall be at APL during contacts, commanding the instrument suite and looking at real-time data products on the EGSE
  - Using the same tools that will have been used throughout I&T to verify instrument functionality
- At least two workstations shall be used per spacecraft; one for command and state of health monitoring, and one for Science displays
  - Allows instrument operator to function independently of science team
- IDPU software is sufficiently modular to allow PLASTIC to command their instrument independently of IMPACT for most operations.
  - PLASTIC has a similar but independent EGSE/POC setup

Operational Constraints

- IMPACT Suite would like to be powered on as soon as possible, subject to spacecraft and other IMPACT constraints
- MAG would like to be powered on before IMPACT boom deployment
- MAG would like boom deployed as soon as possible to get calibration data in the magnetosphere
- MAG requires periodic calibration rolls
- SWEA, STE, SEPT, and SIT covers cannot be opened for at least 24 hours (TBR) after launch to allow spacecraft outgassing
- SWEA and SIT have High Voltage which cannot be operated sooner than 24 hours (TBR) after their doors open
- SIT and SEPT have sunlight avoidance constraints that may delay their cover opening until heliocentric orbit (after the insertion burns are complete and attitude is stable)
- STE cover must be re-closed for off-nominal orientations and thruster firings
- IDPU should be powered on if either SEP or Boom Suite is on.

Normal Operations

- **During Normal Operations, IMPACT will be commanded and monitored from Berkeley**
  - **Using a copy of the EGSE setup**
  - **Limited commanding required; instruments run fairly autonomously**
  - **Routine limit checking and trending run automatically post-pass, with an alarm system to notify an operator (via a pager)**

IMPACT Data Analysis Flow