STEREO IMPACT

Boom Suite Status

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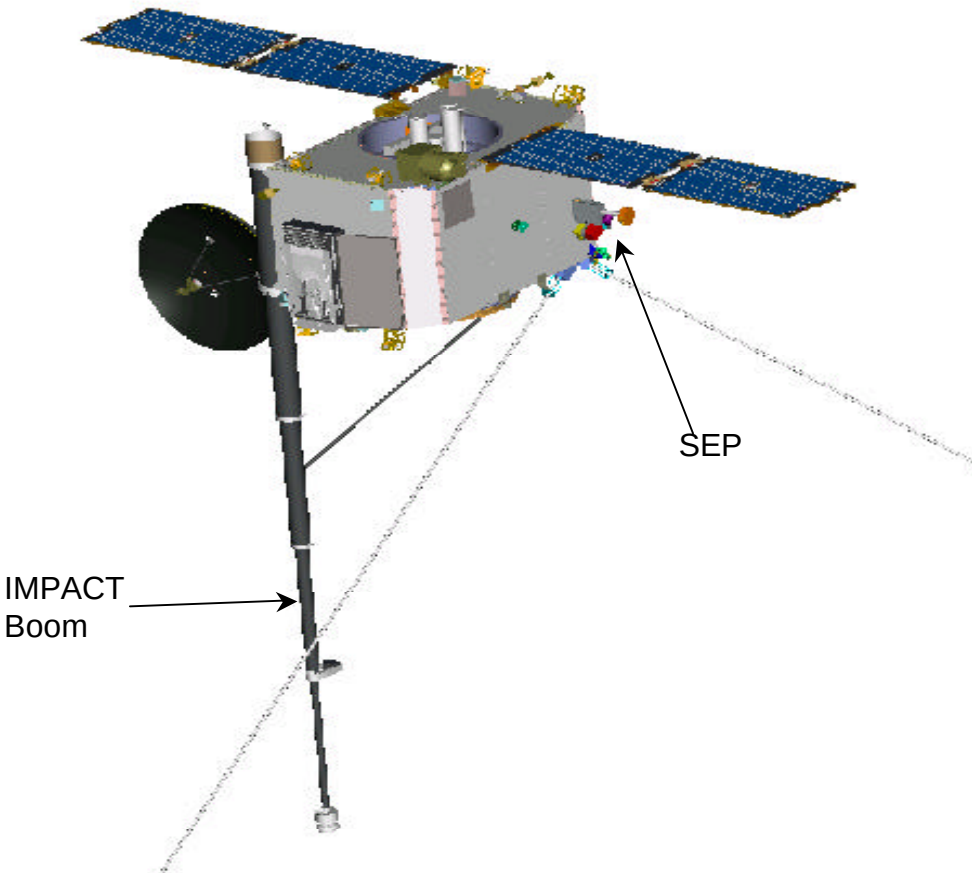
Review History

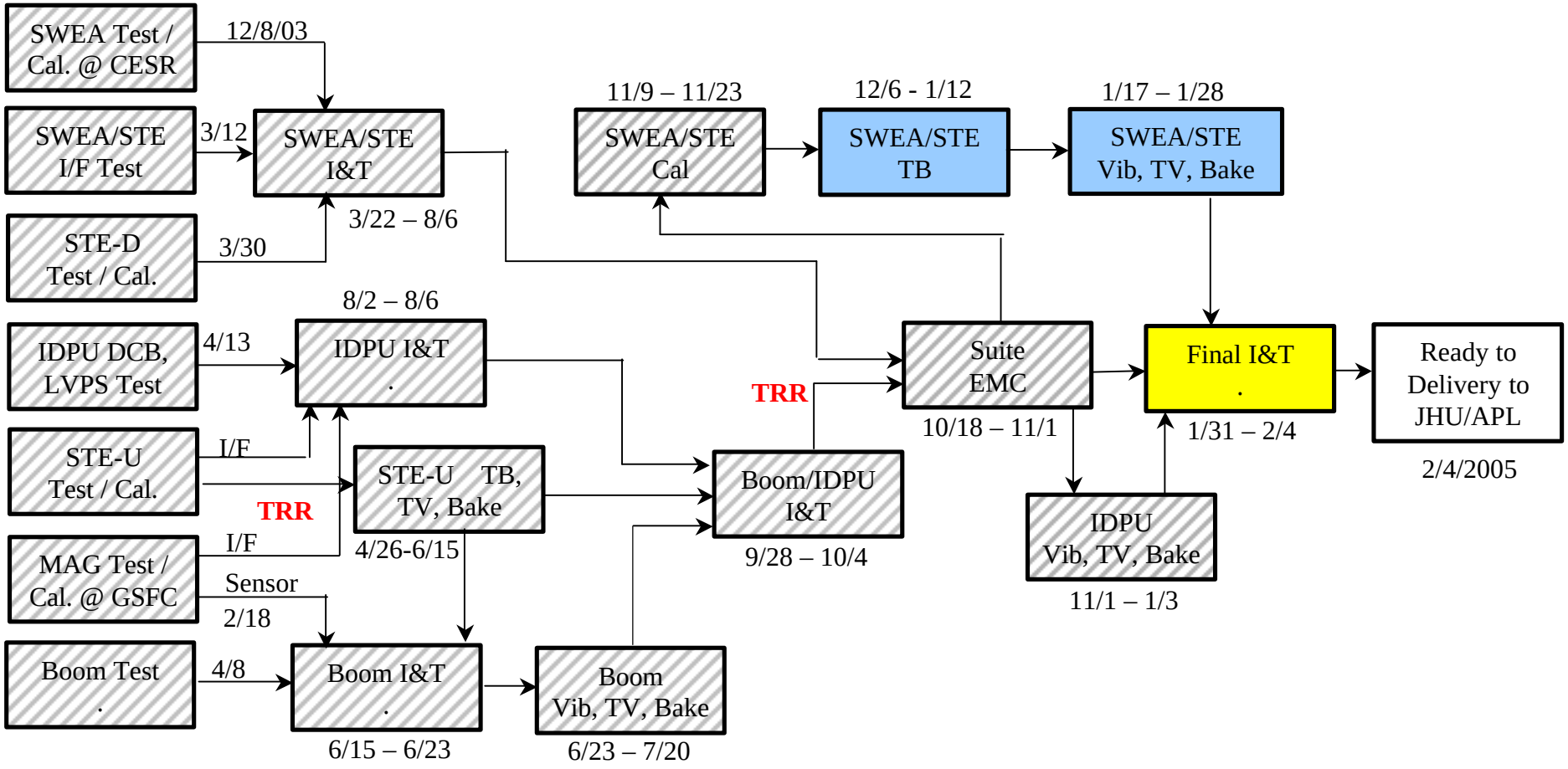
- IMPACT held a suite-level PER in January 2004 to cover general plans and the detailed plans of the first instruments (SEPT)
- A TRR was held in April 2004 to cover the Boom, MAG, and STE-U instrument environmental testing
- A TRR was held in October 2004 to cover the IDPU and SWEA/STE-D environmental testing
- Today's TRR covers the rest of the SEP suite (SEP Central/HET/LET and SIT), which completes the IMPACT suite

IMPACT (In-situ Measurements of Particles and CME Transients) Instrument Overview

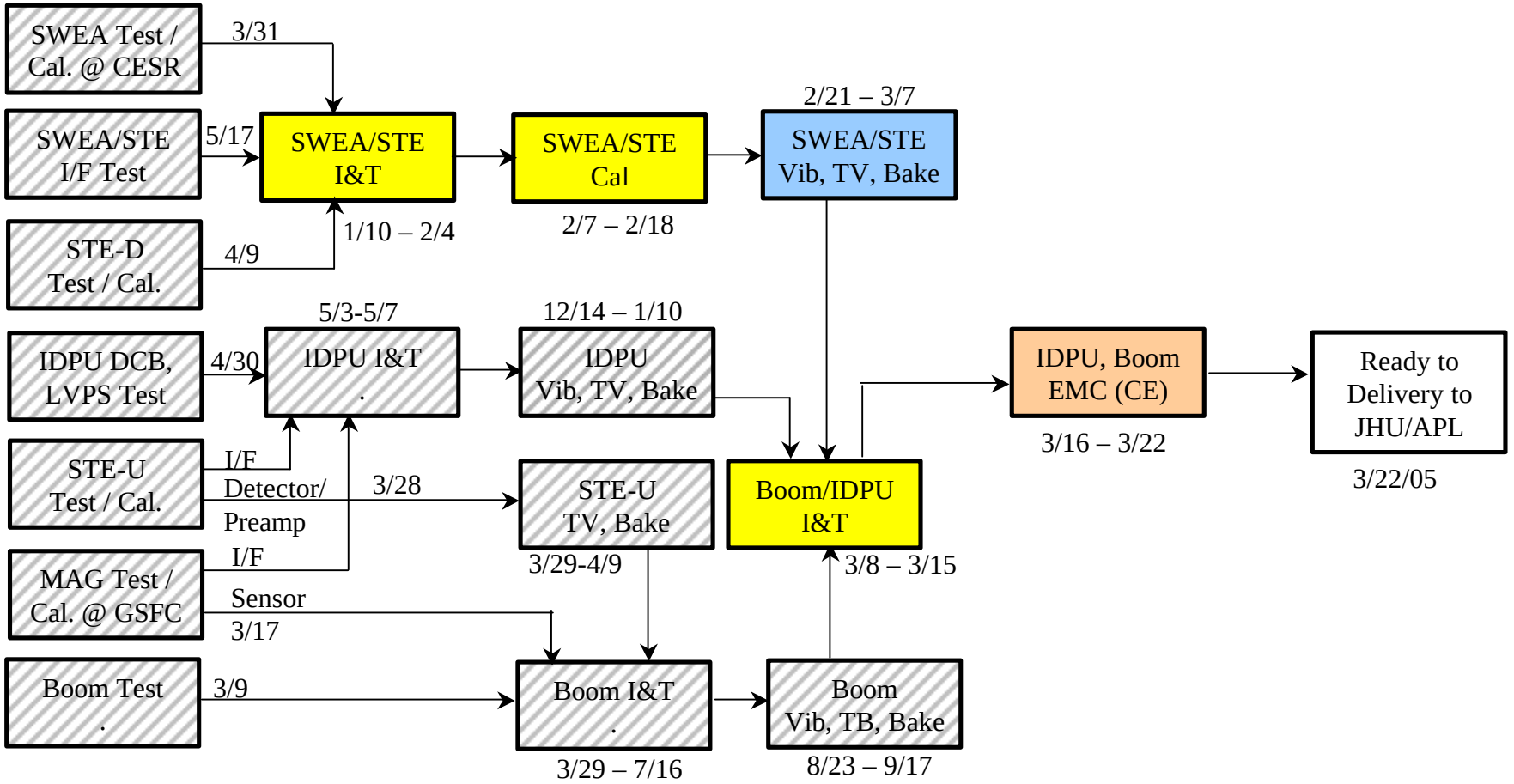
- **Boom Suite:**
  - Solar Wind Electron Analyzer (SWEA)
  - Suprathermal Electron Telescope (STE)
  - Magnetometer (MAG)
- **Solar Energetic Particles Package (SEP)**
  - Suprathermal Ion Telescope (SIT)
  - Solar Electron and Proton Telescope (SEPT)
  - Low Energy Telescope (LET)
  - High Energy Telescope (HET)
- **Support:**
  - IMPACT Boom
  - SEP Central
  - Instrument Data Processing Unit (IDPU)



Boom Suite FM1 Test Flow (1/6/05)



Boom Suite FM2 Test Flow (1/6/05)



Boom Verification Matrix

		Verification Matrix for STEREO/IMPACT/Boom																		Revision Date: 1/6/2004
																				Revision Number: 5
Hardware Description		Test																		
Level of Assembly	Item	Deploy Test, Room Temperatur	Deploy Test, Thermal Vac	Stiffness, Proof Load	Vibration, Sinusoidal	Vibration, Random	Self Shock	Acoustics	Alignment	Force Margin Deployment	Thermal Vacuum	Thermal Cycle	Thermal Balance	End-to-End Conductance Test	EMC/EMI	Magnetics	Bakeout	Deployment Contamination	Contamination Inspection	Comments
C	Proto	C		C																
C	EM	C		C														C		Qual levels
C	PF/FS	C	C	C	C	C	C		C	C	C	C	C	C		C				Protoflight levels
C	FM1	C		C					C					C		C			C	Protoflight levels
C	FM2	C		C					C					C		C			C	Protoflight levels
S	FM1		C		C	C	C				C	C			C		C			Protoflight levels
S	FM2		C		C	C	C				C	C					C			Protoflight levels

Legend:			
Level of Assembly	Unit Type		Status
C = Component	PT =	Prototype	X = Test required
S1 = with MAG, STE-U	PF/FS =	Protoflight / Flight Spare	A = Analysis
S2 - with MAG	FM1 =	Flight unit #1	**C = Test Completed**
S = with all instruments	FM2 =	Flight unit #2	

MAG Test Matrix

		Verification Matrix for STEREO/IMPACT/MAG																	Revision Date: 2005-1-13
																			Revision Number: 2
	Hardware Description	Test																	
Level of Assembly	Item	Elect. test, rm. Temp	Bench Calibration	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Shock	Acoustics	Thermal Vacuum	Voltage margins	Thermal cycle	Thermal balance	>100 hours Operation	EMC/EMI	Magnetics	Bakeout	Contamination	Comments
C	Sensor, EM	C	C																
C	Sensor, F	C	C	C	C	C	C	C		C		C	A	C	C		C	C	Sensor thermal balance by heritage
C	Electronics, EM	C	C	C	C									C					
C	Electronics,F	C	C	C	C	C	C	C		C	C	C		C	C		H	H	

Legend:					
	Level of Assembly	Unit Type		X =	Test required
				A =	Analysis
	C = Component	BB	Breadboard	H =	Test at higher level of assembly
	I = Instrument	EM	Engineering Model		(Boom for sensor, IDPU for electronics)
		PT	Prototype	**C =**	**Test Completed**
		PF	Protoflight		
		F =	Flight		

STE-U Test Matrix

		Verification Matrix for STEREO/IMPACT/STE																		Revision Date: 01/13/2005
																				Revision Number: 3
Hardware Description		Test																		
Level of Assembly	Item	Elect. test, rm. Temp	Bench Calibration	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Self Shock	Acoustics	Thermal Vacuum	Voltage margins	Thermal cycle	Thermal balance	Life Test	EMC/EMI	Magnetics	Beam Calibration	Bakeout	Contamination Inspection	Comments
C	Detector, EM	**C**																		
C	Detector, F	**C**																	**C**	
C	Preamp, BB	**C**	**C**																	
I	Instrument, ETU	**C**	**C**	**C**	**C**				**A**		**C**			**C**			**C**			
I	Instrument, PF (FM1)	**C**	**C**			**C**	**C**	**C**		**C**	**C**		**C**		**C**	X	**C**	**C**	**C**	
I	Instrument, PF (FM2)	**C**	**C**			**C**	**C**	**C**		**C**	**C**				H	X	**C**	**C**	**C**	

Legend:

Level of Assembly	Unit Type		X = Test required
			A = Analysis
C = Component	BB	Breadboard	H = Test at higher level of assembly
I = Instrument	EM	Engineering Model	**C = Test Completed**
	PF	Protoflight	
	F =	Flight	

IDPU Test Matrix

Verification Matrix for STEREO/IMPACT/IDPU — Revision Date: 01/13/2005 — Revision Number: 3

Hardware Description		Test																
Level of Assembly	Item	Elect. test, rm. Temp	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Shock	Acoustics	Pressure change	Voltage margins	Thermal Vacuum	Thermal balance	>100 hours Operation	EMC/EMI	Magnetics	Leak	Bakeout	Contamination	Comments
C	PWB, EM	C	C	C						C			C						
I	IDPU EM	C								C			C	C					EMC CE test on EM
C	PWB, F	C	C	C						C			C						
I	IDPU, FM1	C	C	C	C	C			A	C	C		C	C	X		C	X	EMC at Suite level
I	IDPU, FM2	C	C	C	C	C			A	C	X		C	X	X		C	X	EMC at Suite level

Legend:

Level of Assembly	Unit Type		X = Test required
			A = Analysis
C = Component	BB =	Breadboard	H = at higher level of assembly
I = Instrument	EM =	Engineering Model	**C = Test Completed**
	PT =	Prototype	
	PF =	Protoflight	
	F =	Flight	

SWEA/STE-D Test Matrix

			Verification Matrix for STEREO/IMPACT/SWEA																		Revision Date: 01/13/2005
																					Revision Number: 3
Hardware Description		Test																			
Level of Assembly	Item	Pedestal Interface Tes	Elect. test, rm. Temp	Voltage margins	Bench Calibration	Beam Calibration	Elect. Test, hot	Elect. Test, cold	Vibration, Sinusoidal	Vibration, Random	Self Shock	Acoustics	Thermal Vacuum	Thermal cycle	Thermal balance	Life Test	EMC/EMI	Magnetics	Bakeout	Contamination Inspection	Comments
C	MCP, F		C			C															
C	Preamp, F		C		C																
C	Optocouplers, F		C		C																
S	Electronics, EM		C	C	C		C	C													
S	Electronics, F		C	C	C		C	C											C		
I	Instrument, EM1	C	C	C		C												C			UCB test unit
I	Instrument, EM2		C	C		C						A									CESR test unit
I	Instrument, PF (FM1)	C	C	C		C			X	X	C		X	X	C	X	C	X	C	X	
I	Instrument, PF (FM2)	X	C	C		C			X	X	C		X	X		X	H	X	X	X	

Legend:

Level of Assembly	Unit Type		X = Test required
			A = Analysis
C = Component	BB =	Breadboard	H = Test at higher level of assembly (at UCB)
S = subsystem	EM =	Engineering Model	**C = Test Completed**
I = Instrument	PF =	Protoflight	
	F =	Flight	

Boom Suite Test Results

- **Boom suite tests to date have been successful**
  - **Problem/Failure Report summary below**
    - **All have been reviewed. Most at or near closure.**
  - **Some repeat testing after problem fixes has been required, as negotiated with STEREO Project, generally following GEVS**
  - **Waivers:**
    - **We have the same pre-environmental test waivers we presented back at the April TRR**
    - **We also have an EMC configuration waiver, described in the EMC section**
    - **No post-test waivers required (except EMC – see EMC section).**

Boom Suite PFR Summary

ID #	Description	Assignee	Opened	Closed
1001	Qual boom deployment failure in Thermal Vac	McCauley	2003-08-15	2004-01-07
1002	STE-U Assembly problems (broken bond wire)	Curtis	2004-04-12	2004-06-25
1004	SEP LVPS Middle FM1 Problem	Heavner	2004-04-23	2004-06-08
1005	SEP LVPS Top FM1 Problem	Heavner	2004-04-27	2004-06-08
1006	STE-U FM1 Mis-wire (thermal vac feed-through)	Curtis	2004-04-30	2004-06-25
1007	SWEA LVPS FM1 LTC1877 Failure	Curtis	2004-05-10	
1008	STE-U FM1 Door failure (cold)	Curtis	2004-05-10	2004-06-25
1009	STE-U FM1 preamp oscillations	Curtis	2004-06-14	2004-06-25
1011	STE-U FM1 Door failure (post-vib)	Curtis	2004-06-28	
1012	IDPU FM1 LVPS part failure	Curtis	2004-07-15	
1013	STE-U FM2 door failure (status sense switch)	Curtis	2004-07-27	
1014	STE-U FM2 door failure, actuator burn-out	Curtis	2004-07-30	
1015	SEP FM1 LVPS Middle Board, pin damage	Heavner	2004-07-28	
1016	FM2 Boom Lock Pins, epoxy in the hole	McCauley	2004-08-02	
1017	SEP FM2 LVPS Middle board, wire damage	Heavner	2004-08-05	
1018	SIT FM2 HVPS stack broke	Berg	2004-08-25	
1020	FM2 Boom Actuator Harness	McCauley	2004-09-13	
1021	FM2 SWEA/STE-D Temp Sensor	Curtis	2004-09-27	
1022	SIT FM1 HVPS Stack broke	Curtis	2004-09-28	
1023	SWEA FM1 LVPS Transformer	Curtis	2004-10-04	
1024	SEP FM1 LVPS flex problem	Curtis	2004-10-08	
1025	SEP Intermittents during Suite I&T	Curtis	2004-11-05	
1026	FM2 PLASTIC LVPS short	Heavner	2004-12-1	
1027	FM1 IDPU Thermal Vac D5 Failure	Curtis	2004-11-23	
1028	FM1 SWEA Cold Start	Curtis	2004-12-13	
1029	FM1 SWEA Anode2	Curtis	2004-12-20	
1030	FM1 SWEA Too Cold	Curtis	2004-12-28	
1031	FM2 IDPU Cold Start	Curtis	2004-12-28	

SEP LVPS Issues

- The SEP LVPS were built and tested at UCB, then delivered to Caltech for integration with the SEP Central unit.
- All PFRs addressed with the Project and closed “in principle”
- PFR1004, FM1 Middle Board
  - Problem: Incorrect Signal found in bench test
  - Cause: Layout error
  - Corrective Action: Cut and jump solution applied to both units. Analysis indicates no part over-stress, tested OK.
  - Status: OK to proceed with environments
- PFR1005, FM1 Top Board
  - Problem: No output voltage on two supplies
  - Cause: Design error caused damage to the regulators (negative voltage on Sync)
  - Corrective Action: Modified design to avoid problem, cut and jump onto both flight units, replaced regulators, tested OK
  - Status: OK to proceed with environments

SEP LVPS PFRs, Continued

- **PFR1007, SWEA FM1**
  - **Problem:** LTC1877 regulator failure
  - **Cause:** Part screening stressed parts, resulting in high level of fall-out, latent failures
  - **Corrective Action:** Screening fixture redesigned, new batch screened (no fall-out), parts replaced in all supplies (including SEP FM1 and FM2). No subsequent problems with these parts hundreds of hours of test including TV on some units)
  - **Status:** OK to proceed with environments
- **PFR1015, FM1 Middle Board**
  - **Problem:** Noisy output
  - **Cause:** Layout error
  - **Corrective Action:** Cut-and-jump fix applied to both boards, and stressed part on FM1 replaced, tested OK
  - **Status:** OK to proceed with environments

SEP LVPS PFRs, Continued

- **PFR1017, FM2 Middle Board**
  - **Problem:** Incorrect Output Voltage during unit test
  - **Cause:** Cut-and-jump wire damaged in assembly (too close to mounting hardware)
  - **Corrective Action:** Replace stressed parts, re-route wires. Tests OK.
  - **Status:** OK to proceed with environments
- **PFR1024, FM1 SEP LVPS**
  - **Problem:** Output Voltages Open
  - **Cause:** Output Flex-Strip torn at PWB
  - **Corrective Action:** Rebuild PWB with flexstrip and retest OK; modify procedures to avoid stressing flex strip in test and shipping
  - **Status:** OK to proceed with environments
- **PFR1025, FM1 SEP Restarts – see SEP section**

SIT HVPS Issues

- The SIT HVPS were built and tested at UCB, then delivered to UMd for integration with the SIT instruments
- Two PFRs for SIT HVPS, both relating to mechanical damage in the multiplier stack prior to installing its mechanical support
    - The stack support design has been qualified by previous flight experience
- All PFRs addressed with the Project and closed “in principle”
  - PFR1018, SIT FM2 HVPS
    - Problem: Multiplier Stack broken in assembly
    - Cause: Excessive manipulation of tap wire
    - Corrective Action: Replace Stack, modify procedures, Install stack support, tested OK
    - Status: OK to proceed with environments
  - PFR1022, SIT FM1 HVPS
    - Problem: Multiplier Stack broken in shipment
    - Cause: Should not have been shipped without stack support
    - Corrective Action: Stack replaced, stack support added, tested OK
    - Status: OK to proceed with environments

IMPACT Suite EMC Test Results

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EMC Testing Summary

- EMC tests called out in the Project EMC Requirements document
- Only FM1 gets the full suite of EMC tests
  - Bonding & Isolation
  - CE01, CE03, CE07 (4 power services)
  - CS01, CS02, CS06 (4 power services)
  - RE01, RE02
  - RS03
- IMPACT FM1 Suite performed EMC testing together
  - Tested at EMC Tempest in Anaheim in October 2004
  - Some minor (mostly mechanical) non-flight configuration issues
  - PLASTIC was not available to test with IMPACT – will test separately
  - A Waiver for these differences from the plan was submitted and approved by the EMC committee
- FM2 will get a subset of tests (as called out in the requirements)
  - CE03
  - Will be performed separately for each separately powered subsystem (IDPU, Boom, SEP)

FM1 EMC Test Results

- During the tests regular meetings with the EMC committee were held to discuss and tentatively approve exceedances
  - A formal waiver is in process
  - Passed post-EMC CPT – no damage
- RE01 Exceedances:
  - 15.6KHz, 31.2KHz, 46.8KHz from the MAG drive
  - 19.8KHz, 39.6KHz from SEP (serial interface current?)
- RE02 Exceedances:
  - 24MHz IDPU clock
  - Harmonics of the SEP 32MHz and SEPT 18MHz clocks from 96MHz to 1.5GHz

FM1 EMC Test Results, Continued

- **CE01/03 Exceedances:**
  - **MAG Heater**
    - **50KHz harmonics between 250KHz and 6MHz**
      - **Has been improved by modifying wiring layout and tweaking input filter**
  - **Boom**
    - **172Hz SWEA sample rate**
    - **100KHz LVPS oscillator**
    - **2MHz on interface harness, shift clock**
  - **SEP**
    - **19.8KHz in SEP to SIT harness (serial clock)**
    - **200KHz power converter harmonics, 1.2MHz-10MHz**
      - **Has been improved by tweaking filter**

FM1 EMC Test Results, Continued

- **RS03 Sensitivities**
  - **STE, SIT, SEPT detectors, occasional increased count rate 100MHz-4GHz**
    - **Drops to background at ~6-12dB lower signal**
  - **STE sensitivity continues up to 8.5GHz (Transmit frequency)**
    - **Quiet when we change from harsh AM modulation to more realistic FM modulation**
- **CS01/02/06 Sensitivities**
  - **IDPU**
    - **Some noise in MAG and STE, drops to background at –6dB**
    - **Some 1553 errors (CS06); all handled correctly by the IDPU software**
  - **Mag Heater**
    - **Some noise in MAG and STE, drops to background at –6dB**
  - **Boom**
    - **Some MAG and STE noise, not significant**
  - **SEP**
    - **Some HET/LET detector noise, drops to background at –6dB**