These notes include requirements and suggestions for the ISUAL DPU board PCB layout. The UCB SSL drawing number for this PCB design is 8497, Revision A. The ISUAL DPU board is much like the IMAGE DPU board (drawing number 8102).

GENERAL

1. Technical contact for this design:
   Curt Ingraham, 510 643-7395, ingraham@ssl.berkeley.edu
   Fax: 510 643-8302.
   Alternate contacts:
   Stu Harris, 510 643-3395, sharris@ssl.berkeley.edu
   Bruce Dalen, 510 642-0308, bdalen@ssl.berkeley.edu
2. Related SP design documents:
   a. Schematic, Engineering Model, 8503-V7, Rev. A
   b. BOM, Engineering Model, 8504-X7, Rev. A
   c. DPU PCB Outline, 8505-V7, Rev. C
   d. AEP PCB Outline, 8549-A4, Rev. A
   e. PCB Layout Notes, 8506-W7, Rev. A (this document)
   f. PCB Component Land Geometry, 8743-T1, Rev. C
3. Board layers. Six layers is the minimum, with signal traces on outer layers and power and ground planes on the internal layers as follows:
   Layer 1: Component side; signal traces
   Layer 2: Inner layer; signal traces
   Layer 3: Ground layer; ground plane
   Layer 4: Power layer; +5 V
   Layer 5: Inner layer; signal traces
   Layer 6: Solder side; signal traces

   Additional layers may be added to simplify routing.
4. Pin numbers. U101-3 means pin 3 of U101.
5. N.C. pins. Pins marked "N.C." on the schematic are not to be connected to any other signal or net.
6. Reference designators. C1xx, R1xx, etc are on sheet one of the schematic; C2xx, R2xx are on sheet two; and so on.

PCB ORIENTATION

10. See DPU outline drawing; it is a view of the Component side.
    North: edge near J11.
    South: edge near Pin 62 end of J16.
    East: edge near Pin 8 end of J12.
    West: edge near J10 and J16.
    Component (top) side: side with J10-J12 and J16 (near side in outline drawings).
    Solder (bottom) side: side with J52 body (far side in outline drawings).

MECHANICAL

20. The board outline shall be as shown in the AEP PCB outline drawing. See AEP Outline drawing for details and dimensions of the board corners, mounting holes, and keep-out areas.

21. Except for connectors J10, J11, J12, and J16 and other components noted in these instructions, no components or component side signal traces are allowed in the keep-out area along the four edges of the board.

22. Allow a 0.050-inch safety margin between outer layer signal traces and the keep-out area along the edges of the board.

23. The 8 mounting holes must be as shown. Pads for the mounting holes are allowed in the keep-out area. Connect all mounting hole pads to GND.

24. Traces on all layers except component side may pass through the board edge keep-out area but must clear the edges of the board by at least 0.050 inch.

PLACEMENT

30. Connectors J10, J11, J12, J16, and J52 must be located exactly as shown in the outline drawing.

31. Note that J10, J11, J12, and J16 are on the component side; J52 mounts from the solder side.

32. CPU. Place the CPU (U101) close to J16 at the left edge. Notice that most of the signals from J16 pass straight across to U101.

33. Place oscillator U103 so that U103-8 is close to U102-150.

34. Place thermistor R201 near U209-U212.

35. Place thermistor R202 near R201.

36. Place U209-U212 close to J10.

37. Place R221-R228 and C221-C228 between J10 and U209-U212.

38. Place U302, D301, and Q301 close to U301.

39. Place RN301-RN310 and OPAMPs U303-U307 between U301 and J11. Keep each OPAMP's output traces away from its input traces.

40. Place U402 close to J11.

41. Place L401-L403 as close as possible to J52.

42. Place C414 and C415 close to L402 and L403.

C.A. Ingraham, UCB SSL, +1 510 643-7395, ingraham@ssl.berkeley.edu

43. Decoupling capacitors. Place a power supply decoupling capacitor as close as possible to the power pin of each IC. Each of these capacitors is shown on the schematic. For most ICs, the capacitor has the same reference designator number as its IC. For example, C103 is the capacitor for U103.

For ICs with several power pins (e.g. U102), place each capacitor close to its power pin as implied by its position on the schematic.

J401-J404 are for discrete wire (#24 AWG) connections to off-board heater resistors. Place J401 & J404 near one board edge; place J402 & J403 on the opposite board edge.

ROUTING

50. Ground layer. The entire ground layer is to be the ground signal GND. There are not separate analog and digital grounds.

51. Power layer. Use the power layer to route VCC (+5 V).

52. Use a portion of the power layer or some other layer to route +12 V and -12 V. Use large traces for these power signals.

53. Critical signals. Traces for these digital signals should be as short as possible and be routed away from other signals where possible:

a. OSC (U105-8)
b. CPU_X1 (U102-28)
c. PWR_CLK (U102-153)

54. Spare gate inputs. One section of U401 and two sections of U402 are spare gates whose inputs are grounded through "J_NC" jumpers rather than being connected directly to the ground plane (e.g. J495 at U401-5).

The J_NC jumper is to allow the easy rewiring of a pin which might otherwise be connected to the power or ground layer by its plated-thru hole.

J_NC is to consist of two holes with pads, much like a two-pin component footprint, except that the holes and pads can be smaller and closer (say, 0.1 inch) together; the pads are to be joined by a short, accessible outer-layer trace.

55. Another special jumper, J_1 (e.g. J112 at J16-10), is a similar arrangement for no-connect pins. J_1 is to be one small hole and pad with a short trace to the no-connect component pin.

56. Connect all connector mounting hole pads to GND.

COMPONENTS

60. Use SMD component footprints per PCB Component Land Geometry drawing.

61. Use component footprints as on other ISUAL boards.

62. Coordinate new component footprints with Curt Ingraham or Stu Harris.

63. Notice that U101 is a 40-pin DIP; on 8102 this device was a 42-pin flat-pack.

64. J12 is a 15-pin connector (Positronic SND15F5000G) with pins 9-15 not installed.

65. J52 is to be installed with the body and female contacts on the solder side and the male contacts on the component side as shown by the pin numbers on the DPU outline drawing.

66. Component footprints must accommodate FM components. Where the EM component package is different from the FM component package, try to create a footprint which will work for both.

67. For J101 and J301 allow for a connector body of 0.35 x 1.00-inch.

68. For U103 allow for a 0.54 x 0.89-inch can package.

MISCELLANEOUS

70. Component and solder side silkscreens shall include reference designators.

71. Add this text in copper on the component side:

    ISUAL AEP DPU, ASSY 8502, REV

Leave a blank area after REV in which to hand-write a revision letter.

72. Add this text in copper on the solder side:

    ISUAL AEP DPU, FAB 8497, REV A

73. Use a square pad or silkscreened square on the outer layers to mark pin 1 on connectors, ICs, and resistor networks; to mark the positive end of polarized capacitors; to mark the cathode end of diodes; and to mark the emitter lead of transistors.

C.A. Ingraham, UCB SSL, +1 510 643-7395, ingraham@ssl.berkeley.edu